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THESIS

DESIGN OF A JAMMING SIMULATOR
FOR A BINARY COMMUNICATION SYSTEM

by

Theodoros J. Pantos

December 1984

Thesis Advisor: D. Bukofzer

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Binary PSK and FSK signals were generated, transmitted, and processed by each receiver, and measurements of each receiver's performance were recorded as each system operated in the presence

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of White Gaussian Noise (WGN) as well as in the presence of a combination of White Gaussian Noise and a jammer waveform.

The system's performance is expressed in terms of the probability of receiver error occuring during the transmission of digital information. The results are plotted as receiver Probability of error (P_e) versus Signal-to-Noise ratio (SNR) for fixed values of and Jammer-to-Signal ratio (JSR). Signal and receiver designs are presented and diagrams as well as schematics have been included for clarity.

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Design of a Jamming Simulator for a Binary Communication System.

by

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Submitted in partial fulfillment of the
requirements for the degree of

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December 1984

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Two receivers for coherent Phase Shift Key (PSK) and Frequency Shift Key (FSK) transmission have been designed in order to validate theoretical studies involving jamming of digital communication receivers.

Binary PSK and FSK signals were generated, transmitted, and processed by each receiver, and measurements of each receiver's performance were recorded as each system operated in the presence of White Gaussian Noise (WGN) as well as in the presence of a combination of White Gaussian Noise and a jammer waveform.

The system's performance is expressed in terms of the probability of receiver error occuring during the transmission of digital information. The results are plotted as receiver Probability of error (P_e) versus Signal-to-Noise ratio (SNR) for fixed values of and Jammer-to-Signal ratio (JSR). Signal and receiver designs are presented and diagrams as well as schematics have been included for clarity.

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I. INTRODUCTION

In many communication applications, the detection (or discrimination) of signals in the presence of noise and jamming waveforms is of main importance. Depending on the point of view, the ability of the receiver to detect the transmitted signal or the effectiveness of the jammer in terms of its ability to prevent signal detection can be the focus of interest in the investigation of performance of communications receivers. For binary Phase Shift Key (PSK) and Frequency Shift Key (FSK) modulating systems, the performance of the receiver and the effectiveness of the jammer have been analyzed in Ref.[1]. In this referenced work, the performance of an optimum receiver is analyzed in the presence of an optimum (energy constrained) jamming waveform.

For this thesis, the design and construction of the optimum receiver analyzed in Ref.[2], is carried out and its performance in the presence of an optimum jamming waveform (as derived in Ref.[3]) and additive White Gaussian Noise is measured, examined, and evaluated.

The most important result of this study is that it validates all the theoretical results derived in Ref.[3].

Furthermore it clearly demonstrates (as reported in Ref. 3) that in the presence of an optimum jamming waveform with energy greater than the energy of the signal (JSR > 1), the presence of noise can improve the performance of the receiver. This effect has been observed for such values of JSR when the Signal-to-Noise ratio (SNR) takes on values in the region of -5 to +5 dB.

This report is divided as follows. In Chapter II, the theoretical concepts on which the stucture of the receiver that was analyzed and built is based are presented. Additionally, key results from Ref.[1] are repeated here for clarity. The designed and constructed systems are described in Chapter III, while the experimental results are presented in chapter IV in tabular and diagramatic forms. Chapter V contains the conclusions to be derived from this work, as well as proposals for future work. In Appendix A the schematics of the circuits built are presented.

II. COHERENT CORRELATION RECEIVER

A. GENERAL DESCRIPTION

In binary communication systems, the source (or modulator) transmits one of two signals $s_1(t)$ or $s_0(t)$, over a prescribed time interval. Because in transmission and reception these signals are interfered with by noise, at the receiver one observes the signal r(t) rather than only one of the transmitted signals. Using hypothesis testing concepts, we say that under the hypotheses H_0 and H_1, r(t) takes on the following forms:

$$H_1 : r(t) = s_1(t) + v(t) \qquad 0 \leq t \leq T \qquad (2.1)$$

$$H_0 : r(t) = s_0(t) + v(t) \qquad 0 \leq t \leq T \qquad (2.2)$$

were $s_0(t)$ and $s_1(t)$ are completely known signals and v(t) is a sample function of a Gaussian noise process that is white over a specified bandwidth.

The problem of detecting (or discriminating) signals in the presence of noise, is analyzed using statistical decision theoretic concepts. In digital communication

receivers, of main importance is the probability of bit error. The decision rule (or equivalently, the signal processing algorithm, or the receiver structure) for a minimum probability of error receiver is well documented (see reference 2 for example) and is given by:

$$\int_0^T r(t)s_1(t)dt - \int_0^T r(t)s_0(t) \gtrless \int_0^T [s_1^2(t)-s_0^2(t)]dt + \frac{N_0}{2} \ln \frac{P(S_1)}{P(S_0)} \tag{2.3}$$

where we define

$$\gamma = \frac{N_0}{2} \ln \frac{P(s_1)}{P(S_0)}$$

and $P(s_i)$ is the probability of sending signal $s_i(t)$, for $i=0,1$.

The optimum receiver corresponding to the above decision rule is shown in Figure 2.1, and is known as a correlator receiver due to the correlation performed between the received signal $r(t)$ and the signals $s_1(t)$ and $s_0(t)$.

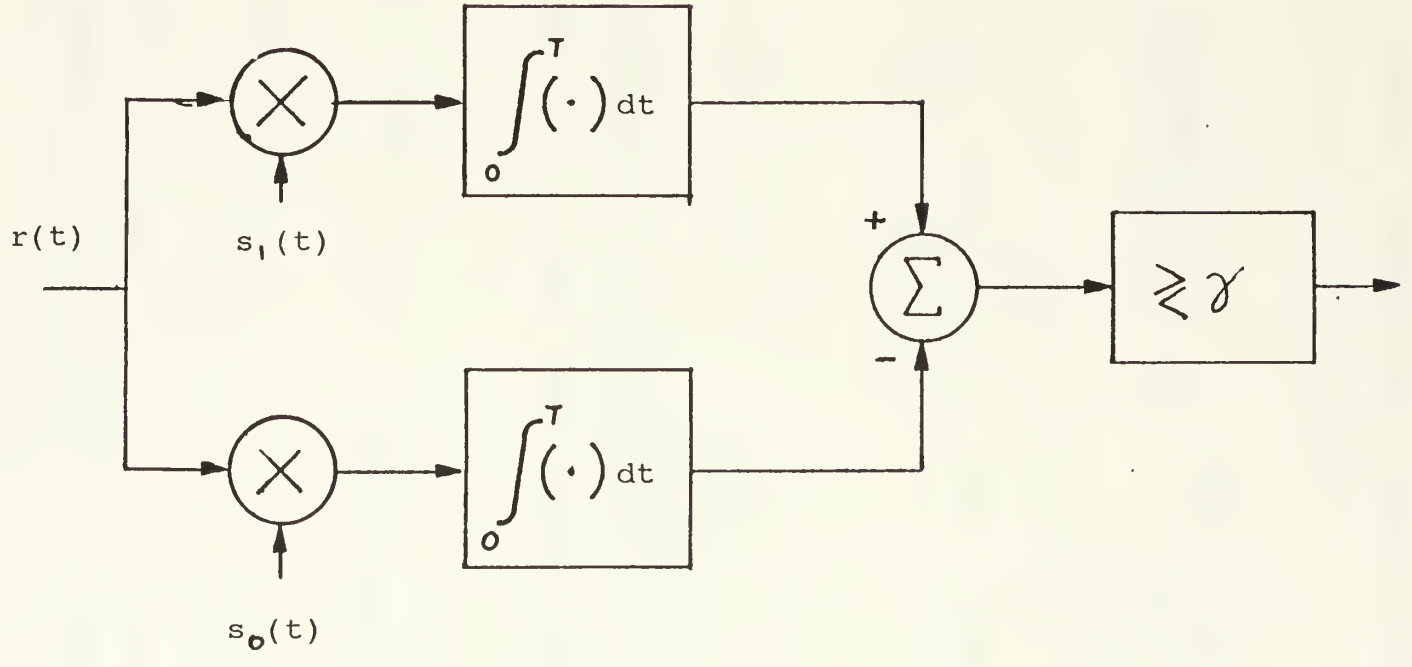

Figure 2.1 Block Diagram of Optimum Receiver

The performance of the receiver is given in terms of the probability of error, which for equally likely prior probabilities (that is, $P(s_1)=P(s_0)=1/2$) becomes

$$P_e = \int_{\sqrt{E(1-\bar{\rho})/N_0}}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-x^2/2}\, dx = \operatorname{erfc}\left(\frac{E(1-\bar{\rho})}{N_0}\right) \tag{2.4}$$

where

$$E = \frac{1}{2}\int_0^T [s_1^2(t) + s_0^2(t)]dt \tag{2.5}$$

is the average energy of the signals $s_1(t)$ and $s_0(t)$ and

$$\bar{\rho} = \frac{1}{E}\int_0^T s_1(t)\cdot s_0(t)dt \tag{2.6}$$

is the normalized signal crosscorrelation

and N_0 (in units of Watts/Hz) is the one-sided power spectral density level of the noise.

The above equation may be written in a simpler form by defining the Signal-to-Noise ratio (SNR) as the ratio of the average energy per bit to the power spectral density level of the noise. Thus, equation 2.4 becomes

$$P_e = \text{erfc}\left(\sqrt{SNR(1-\bar{\rho})}\right) \tag{2.7}$$

There are two widely used choices for $s_0(t)$ and $s_1(t)$ in digital communication applications. One is known as Phase Shift Keying (PSK) in which

$$s_0(t) = -s_1(t) = A\cos w_c t \tag{2.8}$$

and the other is known as Frequency Shift Keying (FSK) in which

$$s_1(t) = A\cos(w_c + \Delta w)t \tag{2.9}$$

$$s_0(t) = A\cos(w_c - \Delta w)t \tag{2.10}$$

For PSK and FSK modulated signals, the above receiver performance expression (see equation 2.5) becomes

$$\text{PSK}: \quad P_e = \text{erfc}\left(\sqrt{2SNR}\right) \tag{2.11}$$

$$\text{FSK}: \quad P_e = \operatorname{erfc}\left(\sqrt{\text{SNR}}\right) \tag{2.12}$$

B. JAMMING OF COHERENT RECEIVERS

In many instances, the received signal is interfered by not only noise but also by a jamming waveform. Thus, the received signal r(t), using hypothesis testing concepts can be represented as

$$H_1 : r(t) = s_1(t) + v(t) + n_j(t) \qquad 0 \leq t \leq T \tag{2.13}$$

$$H_0 : r(t) = s_0(t) + v(t) + n_j(t) \qquad 0 \leq t \leq T \tag{2.14}$$

where now $n_j(t)$ is the jamming waveform. The jamming waveform is modeled as deterministic, yet unknown to the receiver.

The additional interference of the transmitted signal by the jammer has the net effect of increasing the receiver probability of error. The energy P_{n_j} of the jamming waveform is defined as

$$P_{n_j} = \int_0^T n_j^2(t)dt \tag{2.15}$$

A jammer waveform is said to be "optimum" if it maximizes the receiver probability of error subject to a constraint on P_{η_j} .

In Ref.[1], it has been demonstrated that if P_{η_j} is constrained, the jammer that is optimum, i.e. the jammer that causes the maximum increase in receiver probability of error, is

$$n_j(t) = K[s_1(t) - s_0(t)] \tag{2.16}$$

where K is a constant of proportionality that must be set such that the constraint on P_{η_j} is satisfied.

Use of this jammer leads to a receiver probability of error P_e given by

$$P_e = \frac{1}{2}\left\{\operatorname{erfc}\left[\sqrt{E(1-\bar{\rho})/N_o} - 2\sqrt{P_{\eta_j}/N_o}\right] + \operatorname{erf}\left[2\sqrt{P_{\eta_j}/N_o} - \sqrt{E(1-\bar{\rho})/N_o}\right]\right\} \tag{2.17}$$

or in simpler form

$$P_e = \frac{1}{2}\left\{\operatorname{erfc}\left[\sqrt{SNR}\left(\sqrt{1-\bar{\rho}} - \sqrt{2JSR}\right)\right] + \operatorname{erf}\left[-\sqrt{SNR}\left(\sqrt{1-\bar{\rho}} + \sqrt{2JSR}\right)\right]\right\} \tag{2.18}$$

where SNR= E/N_o, and JSR= P_{nj}/E . For the specific cases of PSK and FSK modulation, Equation 2.16 becomes

$$\text{for PSK :} \quad n_j(t) = Ks_1(t)$$

$$\text{and for FSK :} \quad n_j(t) = K[s_1(t) - s_0(t)]$$

For PSK and FSK we have $\bar{\rho}=-1$ and $\bar{\rho}=0$ respectively, so that the receiver probability of error becomes

$$P_e = \frac{1}{2}\left\{\text{erfc}\left[\sqrt{2\text{SNR}}\left(1+\sqrt{\text{JSR}}\right)\right] + \text{erf}\left[-\sqrt{2\text{SNR}}\left(1-\sqrt{\text{JSR}}\right)\right]\right\} \tag{2.19}$$

for PSK and for FSK

$$P_e = \frac{1}{2}\left\{\text{erfc}\left[\sqrt{\text{SNR}}\left(1+\sqrt{2\text{JSR}}\right)\right] + \text{erf}\left[-\sqrt{\text{SNR}}\left(1-\sqrt{2\text{JSR}}\right)\right]\right\} \tag{2.20}$$

III. EXPERIMENTAL PROCEDURE

The design of the receivers and the measurement of their performance are the critical issues in the experimental work undertaken. The design of the systems is based on theoretical results from statistical communication theory discused in Chapter II. The system has to obey constraints consistent with assumptions made in the analysis and derivation of coherent receivers. These constraints make the circuit more complicated than these dictated strictly by theoretical considerations.

Once the design of the systems has been completed, measurements on the probability of receiver error are made using PSK and FSK modulated signals, in order to compare the performance of the designed receivers to the predicted performance based on theoretical results. Measurements that confirm theoretical predictions would signify having achieved properly operating receivers.

A. SYSTEM DESCRIPTION

In order to fullfill the overall constraints, the systems have been designed to consist of a signal generating

circuit, a demodulator, a receiving circuit and an error counting circuit. The first such circuit generates the signals to be transmitted. These signals are fed to the modulator circuit. For this work, two modulation techniques have been used, namely Phase Shift Keying (PSK) and Frequency Shift Keying (FSK).

The modulated signals are sent to the receiver circuit, where a jamming waveform and White Gaussian Noise (WGN) are added to the transmitted signals. This combination of jammer, noise, and modulated signal is fed to the input of the demodulating circuit where the digital information is recovered.

The recovered digital signal is then fed to the counting circuit which is used to compare the transmitted digital information to the received or recovered digital signal and counts how many demodulation errors due to noise and jamming effects have occured.

A general block diagram of the systems implemented is shown in Figure 3.1 Each element of this system is discused in detail next.

1. Signal Generating Circuit

The signal generating circuit produces a bipolar pseudorandom sequence having a period of 127 bits. This

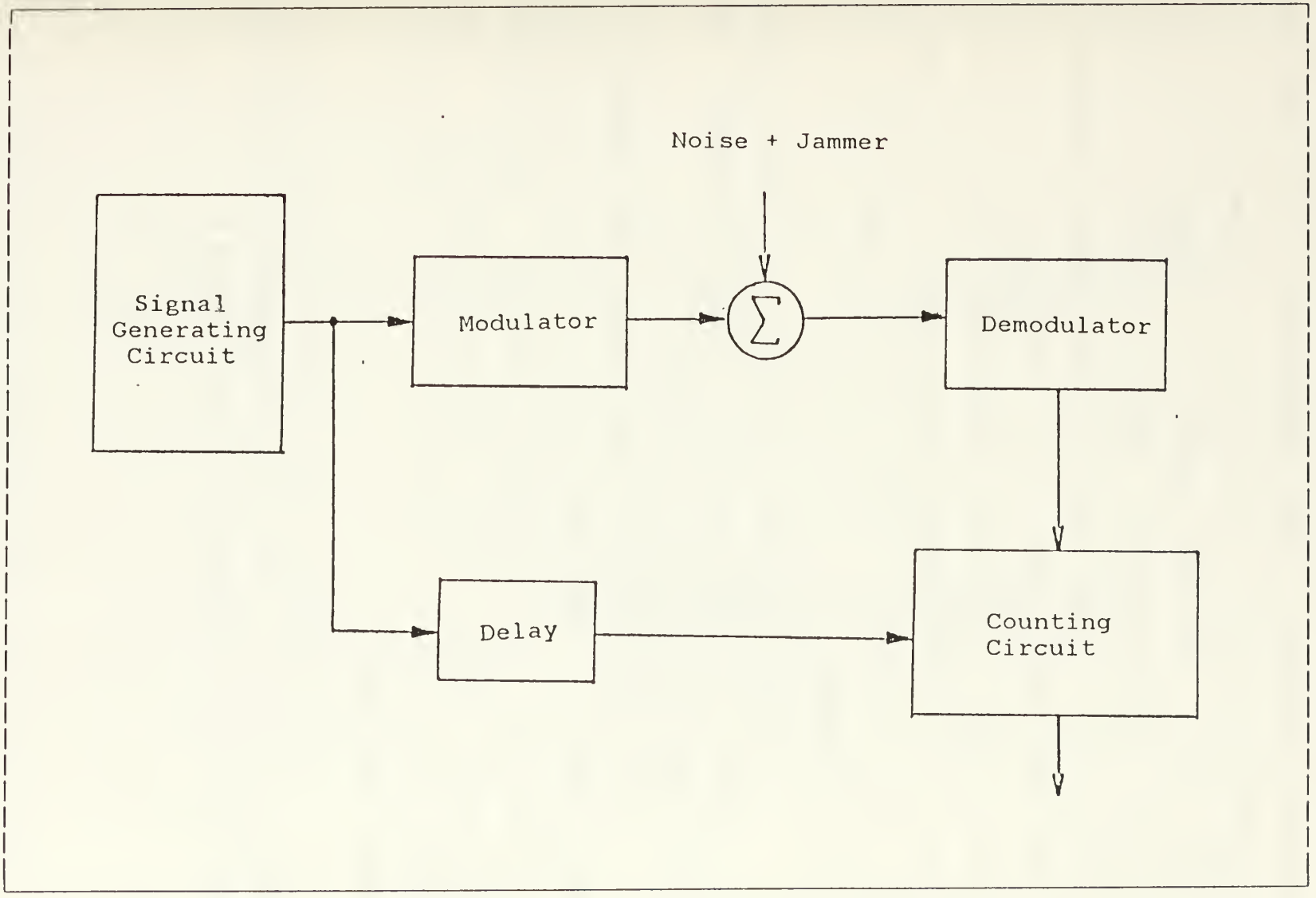

Figure 3.1 Block Diagram of the Implemented System

sequence is produced by a 7-stage shift register with a feedback consisting of the Exclusive-Or of its sixth and seventh stage outputs. The sequence is repeated every 127 clock cycles. The shift register is clocked by the output of a zero-crossing detector which is followed by a divide-by-ten counter. The input to the zero crossing detector is a sinusoidal waveform which is to be modulated by the pseudorandom signal. With this arrangement, the period of the clock is ten times greater than the period of the carrier, and the bit rate is exactly ten times smaller than the carrier frequency.

The signal sequence produced by the shift register is unipolar. A level shifter is used to transform the signal sequence into a bipolar format.

For synchronization requirements in the receiver, a pulse signal is generated using a triggered monostable multivibrator. This produces a very short duration pulse just before the end of the duration of each bit. This synchronizing signal is also converted to a bipolar format using a level shifter.

A block diagram of the signal generating circuit is shown in Figure 3.2 while the corresponding circuit schematic is shown in Appendix A. (see Fig. A.1)

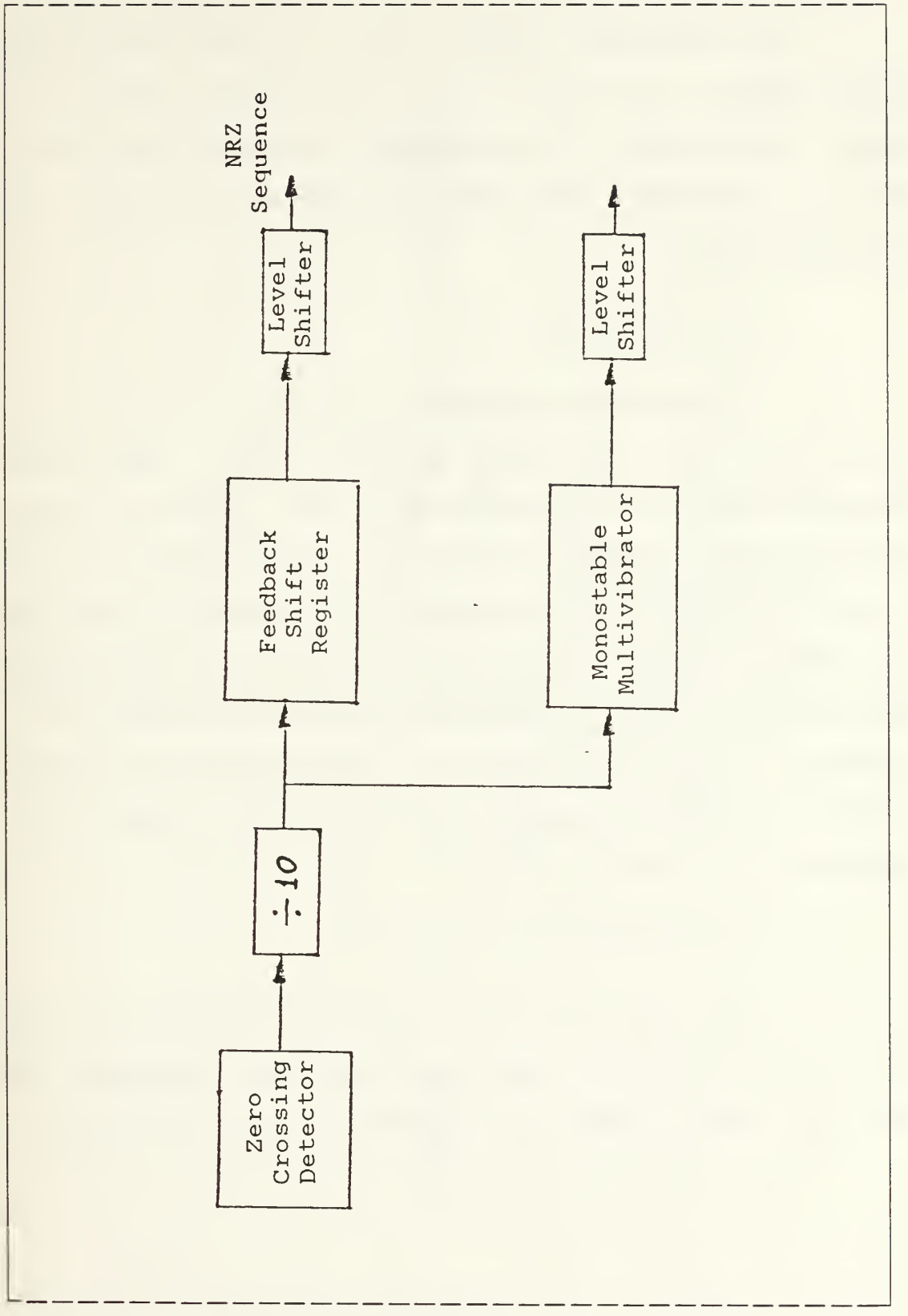

Figure 3.2 Signal Generating Circuit

2. Modulating Circuit

The modulating circuit uses as its input the pseudo-random sequence of bits in order to modulate the carrier before transmission. Two different techniques (for PSK and FSK) are applied, and their corresponding circuits are described below.

a. PSK Modulator

A sinusoidal waveform $A\cos w_c t$ is used as the carrier and the non-return to zero (NRZ) pseudorandom sequence modulates the amplitude of this carrier producing the desired PSK signal. An analog voltage multiplier (AVM) is used to perform this modulation, followed by an amplifier in order to adjust the amplitude of the modulated signal. The modulated signal is therefore of the form $-A\cos w_c t$ or $+A\cos w_c t$. The block diagram of the modulator is shown in Figure 3.3 and the schematic of the circuit is presented in Appendix A. (see Fig. A.2)

b. FSK Modulator

Two sinusoidal wave forms of frequencies f_1 and f_0 are now modulated by the pseudorandom data sequence. The data is a unipolar NRZ sequence, and is fed to two paths.

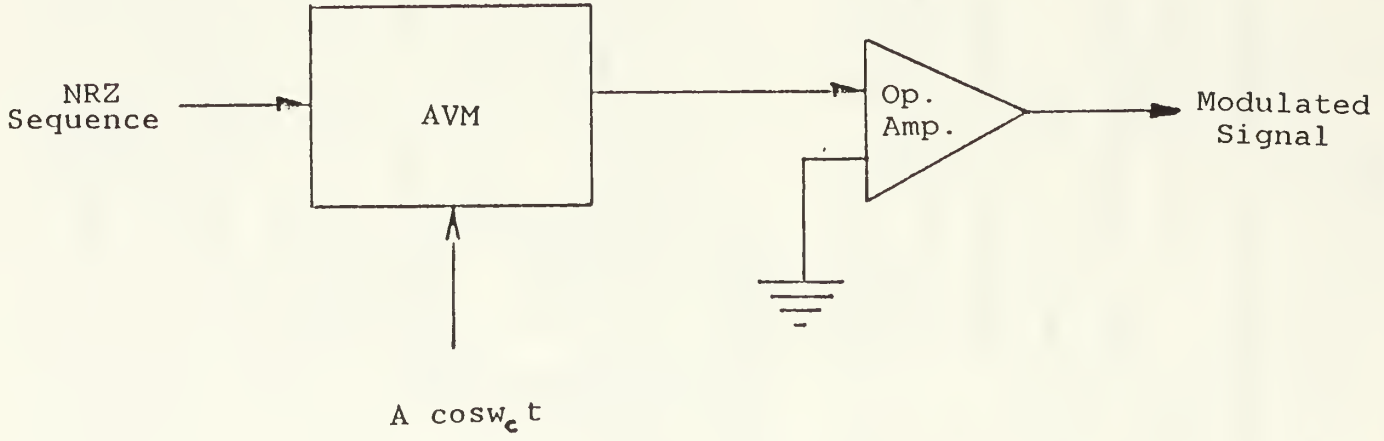

Figure 3.3 PSK Modulator

In the first path an AVM multiplies $A\cos w_1 t$ with the unipolar data. Whenever the data is not zero, the output is simply $A\cos w_1 t$. In the second path the NRZ sequence is inverted and then multiplied by $A\cos w_0 t$. The two paths are then fed to a summer/amplifier producing at the output the FSK modulated signal. In this form, the modulator produces $A\cos w_1 t$ whenever the NRZ sequence is non zero, and $A\cos w_0 t$ whenever the NRZ sequence is zero. The amplitude of the modulated signal is adjusted by an amplifier, as shown in the block diagram of Figure 3.4. The schematic of the circuit is also shown in Appendix A. (see Fig. A.3)

3. Demodulating Circuit

The modulated (information) signal is interfered by a jamming waveform and Gaussian noise before being processed by the demodulating circuit. In order to simulate the interference conditions, the jamming waveform and the noise are added to the modulated signal in two steps using summing amplifiers. In the first step, the jammer waveform is added to the modulated signal, while in the second step noise is added to the sum of the modulated signal and the jammer waveform. The resulting signal is similar to that actually received by a demodulator operating in a noise plus jamming

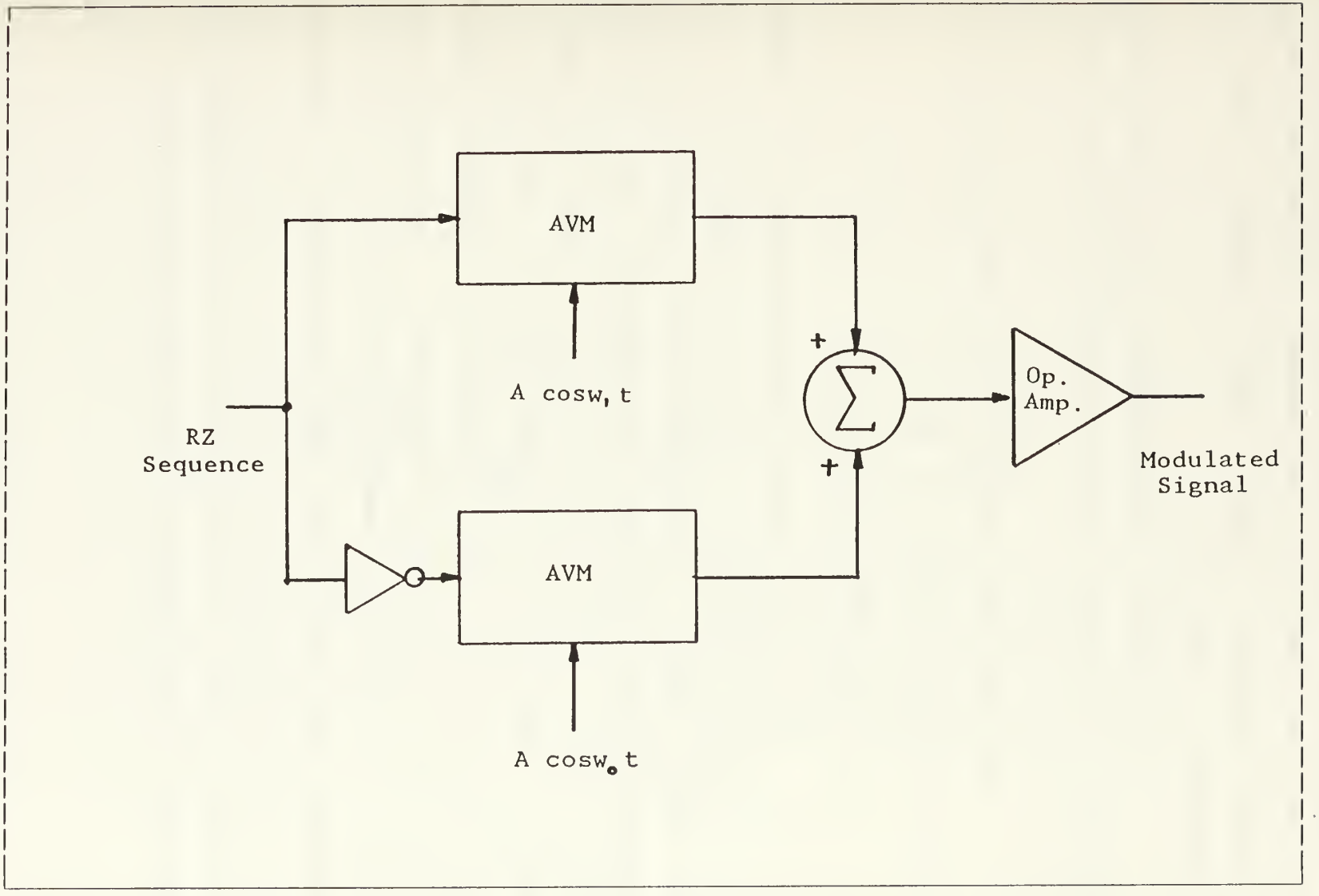

Figure 3.4 FSK Modulator

environment. The demodulators used for PSK and FSK transmissions are based on theoretical results on optimum receivers operating in additive white Gaussian noise only, as described in Chapter II.

An alternative (but equivalent) form of the receiver of Figure 2.1 is used, and this is shown in Figure 3.5 where $s_d(t) = s_1(t) - s_0(t)$.

The demodulating circuits for PSK and FSK modulated signals are now described.

a. PSK Demodulator

The received signal is multiplied in an AVM by the difference signal $s_d(t)$ which for PSK modulation is just the carrier signal. The output of the AVM is fed to an integrator which performs the integration of its input signal during a period of time labeled by the end points t_o and t_f. Here t_o is the starting time of a bit and t_f is a time just before the end of the same bit, which corresponds to the start of the synchronizing pulse. The synchronizing pulse is of very short duration (about 5% of an active bit's duration), and starts before the end of the bit's duration while ending synchronously with the bit. This pulse is used in order to close a digital switch so as to discharge the capacitor of the integrator before the next bit starts.

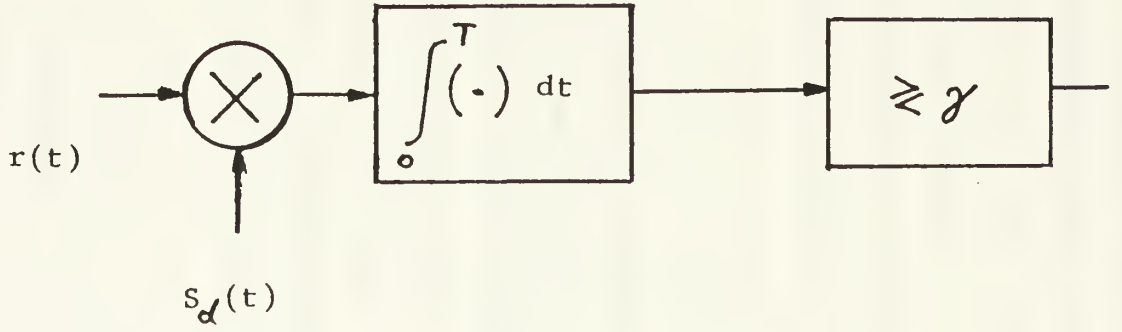

Figure 3.5 Alternative Form of the Receiver of Figure 2.1

This capacitor "dumping" is necessary so as to reinitialize the integrator before the next integration interval begins. The output of the integrator is then compared to a threshold voltage using a comparator and the output of the comparator is sampled at time t_f using a D-Flip-Flop clocked by the synchronizing pulse. The output of the Flip-Flop corresponds to the decisions made by the receiver or equivalently to the decoded digital data. Amplifiers are included in the demodulating circuit placed between the above described circuit stages for signal level adjustment purposes, as is shown in the schematic diagram in Appendix A. (see Fig. A.4)

b. FSK Demodulator

The structure of the demodulator is based on the diagram of Figure 3.5 just as is the case for the PSK demodulator previously described. However, the FSK demodulator is more complicated because the difference signal $s_d(t)$ must be produced as the difference of the two carrier signals $s_1(t)$ and $s_o(t)$ or equivalently, the difference of $\sin w_1 t$ and $\sin w_o t$. This difference signal is generated using operational amplifiers.

The received signal r(t) is multiplied by the difference signal $s_d(t)$ using an AVM and the product of these two signals is integrated over the interval from t_o to t_f using an integrate-and-dump circuit similar in design and

operation as that described for the PSK demodulator. A comparator device compares the output of the integrator to the threshold γ and the comparator's output is sampled at the end of each integration interval t_f using once again the previously described synchronizing signal. The schematic of the FSK demodulating circuit is shown in Appendix A. (see Fig. A.5)

4. Counting Circuit

The signal recovered by the demodulator is now a digital stream corresponding to the transmitted digital information, provided no demodulation errors have occured. In order to determine if any such errors occured, the demodulated digital stream is compared to the transmitted digital "message" in the first stage of a counting circuit. In order to overcome the problem of propagation delays of the demodulated digital message, the transmitted digital message is sampled synchronously with the decision making circuit of the demodulator. This is accomplished using a D-type Flip-Flop clocked by the synchronizing pulse train previously described. The synchronized transmitted and received messages are compared bit-by-bit using an Exclusive-Or operation. The product of the X-ORed digital streams is one pulse for each bit error in the demodulated digital message. A counter is used to count how many such

bit errors occured during the transmission of a message of fixed length. A second counter is used to set the length of the messages for which the number of errors is to be recorded. A signal from this counter is used also to reset the complete counting circuitry after many counting cycles have been completed. The number of counted errors is stored in a shift register and upon the completion of a fixed length message, it records its contents using seven-segment displays. Details of this counting circuit are shown in the schematic of Fig. A.6 in Appendix A.

B. SYSTEM OPERATION

The operation of the system is supported by ±15 volts DC and ±5 volts DC external power supplies. The application of supply voltages to the system is accomplished through voltage regulators in order to obtain the best possible performance of each particular electronic component used. The supply voltages used in each of the system components are shown in the circuit schematics in Appendix A.

1. Choice of Signals and Carrier(s)

For this binary communication system set-up, the signals $m_1(t)$ and $m_0(t)$ as shown in Figure 3.6 are chosen in order to transmit the digital information.

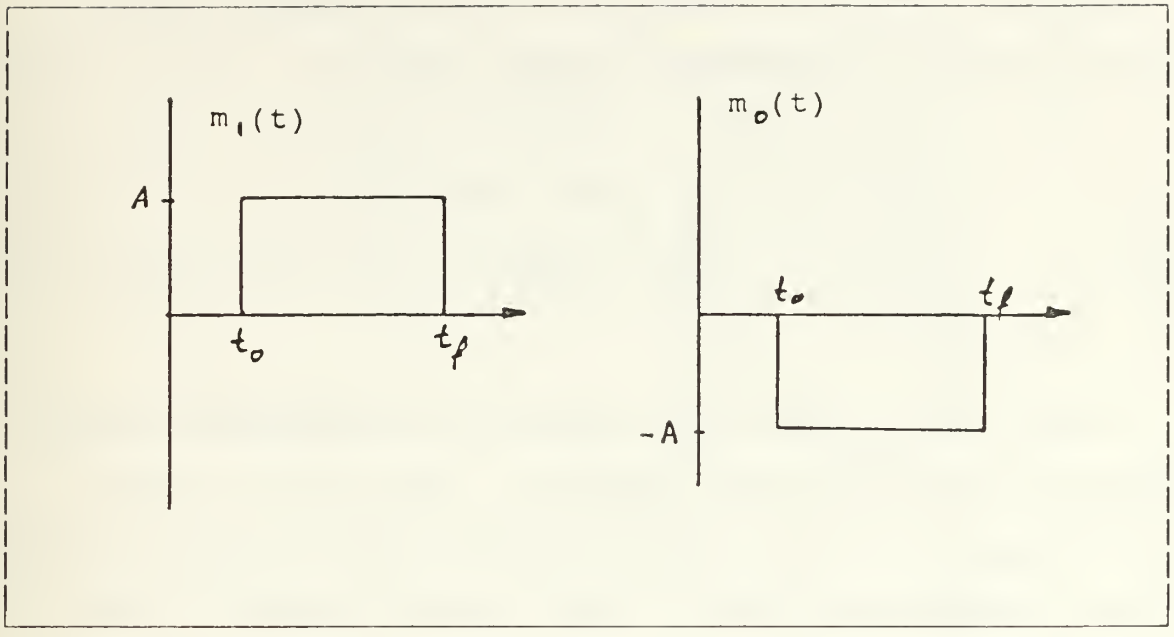

Figure 3.6 Signals Transmitted

The amplitude A of these signals is set to be 5 volts, and the time duration $T_b = t_f - t_o$ is 0.5 msec. Thus the digital signal transmission is performed at a bit rate of 2,000 bits/sec.

The above choice of $m_1(t)$ and $m_o(t)$ has the advantage of resulting in signals $s_1(t)$ and $s_o(t)$ having cross-correlation $\bar{\rho}$ (defined in chapter II) equal to -1. This produces optimum system performance in terms of the receiver probability of error. This can be observed from Equation 2.5 which has been repeated here for convenience,

$$P_e = \text{erfc}\left(\sqrt{SNR(1-\bar{\rho})}\right) \qquad (3.1)$$

Also, since the signals have equal amplitudes and duration, their energies are equal. That is

$$\int_0^T m_1^2(t)dt = \int_0^T m_0^2(t)dt = \int_0^T A^2 dt = A^2 T \qquad (3.2)$$

The digital data to be transmitted is simulated by a pseudorandom maximal length sequence. Thus the two signals $m_1(t)$ and $m_0(t)$ have near equal probabilities of occurence. Such an assumpion was made in the analysis leading to the derivation and evaluation of the receiver performance as specified by Equation 3.1. Thus, the threshold voltage defined by Equation 2.3 and appearing in the receiver structure of Figure 2.1 has to be set equal to zero.

For PSK modulation, only one carrier signal is required. A carrier of amplitude A = 5 volts and frequency of 20 kHz is chosen in order to have ten carrier periods per bit duration which is a minimum required from a practical standpoint. The structure of the clock generator circuit which is part of the signal generating circuit guarantees that exactly ten periods of the carrier are modulated by each bit of data. Thus the modulated signal is of the form

$A\cos w_c t$ when $m_0(t)$ is to be transmitted or

$-A\cos w_c t$ when $m_1(t)$ is to be transmitted.

For FSK modulation, the carrier is frequency modulated in such a way that only two different frequencies, f_1 or f_0 occur, depending on which of the signals $m_1(t)$ or $m_0(t)$ is to be transmitted. The general mathematical expression of FSK modulated signals is

$$s_0(t) = A\cos(w_c+\Delta w)t \tag{3.3}$$

and

$$s_1(t) = A\cos(w_c-\Delta w)t \tag{3.4}$$

Thus the two frequencies are $f_0 = f_c + \Delta f$ and $f_1 = f_c - \Delta f$. The experimental set-up being described sets the lower frequency f_1 to be 20 kHz for synchronization purposes. Because most analysis results require the two signals $s_1(t)$ and $s_0(t)$ to be orthogonal (i.e. $\tilde{\rho}=0$), with non-overlaping power spectral densities, the frequency f_0 is chosen to be 32 kHz. This results in a signal power spectrum arrangement as shown in Figure 3.7.

Two sinusoidal signal generators are used in order to provide the desired signals. The modulated signals are $A\cos(w_c \pm \Delta w)t$ where $f_c = 26$ kHz and $\Delta f = 6$ kHz.

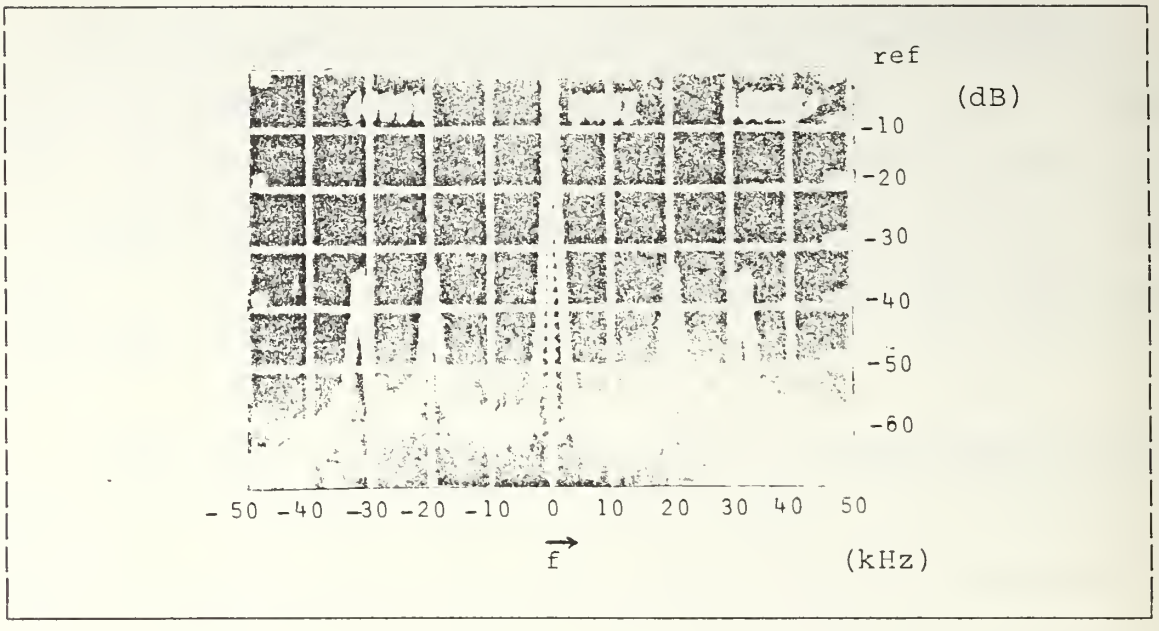

Figure 3.7 FSK Signal Power Spectrum

2. Timing and Adjustment Procedure

Of main importance in this experiment is the signal timing procedures. Any residual signal phase may reduce the overall system performance. Undesirable results are also observed if any of the signals is distorted or is offset by any amplifier. Care must be taken so that saturation of the amplifiers does not occur as this also is a source of reduced system performance.

The clocking waveform generated by the zero crossing detector and followed by a divide-by-ten counter is guaranteed to have equal "high" and "low" intervals, by separating

the divide-by-ten counter into a divide-by-five counter followed by a flip-flop. Thus any DC offset or reference bias in the zero crossing detector does not affect the symmetry of the clocking waveform.

The synchronizing waveform is generated by a monostable multivibrator driven by the clocking waveform. Thus the synchronizing and clocking waveforms are jointly synchronized. This insures proper operation of the integrate and dump circuit. The duration of the synchronizing pulses is very important because the integration time is

$$T_i = T_b - T_s \tag{3.5}$$

where T_b is the bit duration and T_s is the synchronizing pulse duration.

The resulting reduced integration time diminishes the performance of the receiver because the theoretical analysis of the optimum receiver assumes an integration time extending through the entire bit length. If z represents the ratio of T_s over T_b, then the performance of the receiver for equaly likely signals $s_1(t)$ and $s_0(t)$ received in the presence of additive white Gaussian noise is given by

$$P_e = \operatorname{erfc}\left(\sqrt{2SNR(1-z)[1+\operatorname{sinc}2w_c T(1-z)]}\right) \tag{3.6}$$

For the present experiment, z is less than 5% and its effect on performance can be assumed to be negligible.

In order to prevent any signal distortion due to rapidly changing signals, a high slew rate operational amplifier is used throughout the system operating near but never above saturation.

The inputs to the analog voltage multipliers (AVM) used in this experiment were adjusted using amplifiers.

C. MEASUREMENT PROCESS

1. Power of Signal, Noise and Jammer

The consideration of signal power is the single most important issue in this experiment as the accuracy of the measurements of signal, noise and jammer powers directly affects the receiver performance measurements results.

Care must also be taken to insure that limitations in the measurement equipment do not adversely affect performance results.

The measurements are taken using a true RMS voltmeter which performs the measurement: $V_{RMS} = \sqrt{V_{AC}^2 + V_{DC}^2}$.

2. Signal-to-Noise Ratio (SNR) and Jammer-to- Signal Ratio (JSR)

Based on the power measurements, SNR and JSR are calculated. The procedure for these calculations follows from the definition of SNR and JSR given in Chapter II.

For calculations of the SNR, measurements of the signal power alone and of the sum of signal and noise are taken. The energy per signal bit is calculated as

$$E_b = V_s^2 \cdot T_b \qquad (3.7)$$

where V_s is the RMS voltage of the signal and T_b is the bit duration.

The power spectral density level of the noise is calculated as

$$N_o = \frac{V_{s+N}^2 - V_s^2}{BW} \qquad (3.8)$$

where V_{s+N} is the RMS voltage of the sum of the signal and noise and BW is the 3dB noise bandwidth, which for the present case is measured to be 87 kHz. The choice of this bandwidth was partly dictated by equipment availability.

The SNR is then calculated in dB as

$$(SNR)_{dB} = 10\log(E_b/N_o) \qquad (3.9)$$

The JSR is calculated as the ratio of RMS voltages of jamming over signal. When measurements of the receiver performance in the presence of a jammer are taken, the JSR is maintained constant as the SNR is allowed to vary over the range from about -10 dB to 20 dB.

IV. EXPERIMENTAL RESULTS

A. MEASUREMENT PROCESS

In order to evaluate the performance of the system while transmitting a pseudorandom (data) sequence, measurements are taken at the receiver front end involving the signal's rms voltage under two conditions. First, the case in which only the signal is present is considered and second the case in which signal plus additive noise is present is considered.

The Signal-to-Noise ratio (SNR) is calculated using the measurement process as described in Chapter III, given that the data transmission has a constant bit rate of 2,000 bits per second, and the bandwidth (BW) of the additive noise is approximately 87 kHz.

A jamming waveform is then applied to the transmitted signal, and new measurements are taken keeping the Jammer-to-Signal ratio (JSR) constant in order to evaluate the performance of the system in presence of noise and jamming.

For the PSK modulated signal, the jamming waveform used is the sinusoidal waveform of same frequency as the carrier.

Therefore $n_j(t)$ is derived directly from the carrier and mathematically is given by

$$n_j(t) = A\cos w_c t$$

For the FSK modulated signal, the jamming waveform is generated by difference amplifiers as the difference of the two carrier sinusoidal waveforms $A\cos w_1 t$ and $A\cos w_0 t$. Thus

$$n_j(t) = A\cos w_1 t - A\cos w_0 t$$

The choice of these waveforms as jamming waveform is based on the results of Ref.[1] and the discusion at the end of Chapter II.

Tables and figures of the measured performance of PSK and FSK modulating techniques are presented in the next sections.

B. PSK EXPERIMENTAL RESULTS

For PSK modulation the performance of the system in the presence of noise and the jamming waveform described in Section A of this Chapter in terms of the probability of receiver error is calculated as the SNR changes for specified values of JSR. The results are shown in Tables 4.1 and 4.2 as JSR takes on the values 0.0, 0.5, 1.0, 2.0 and 5.0. In Figures 4.1 through 4.5 the probability of error (P_e) versus SNR for the corresponding values of JSR is plotted.

In Figure 4.1 the performance of the receiver is plotted for the case when the transmitted signal is interfered by noise only. (That is, there is no jamming waveform present.) The solid line represents the theoretical performance of the receiver which is calculated from Equation 2.11. The small triangles represent the measured values of the performance for the designed receiver. These values are also presented in Table 1.

In Figures 4.2 through 4.5, the performance of the receiver is plotted when the transmitted signal is interfered by noise as well as by the jamming waveform previously described. Each of the Figures corresponds to a specified value of JSR. The solid line represents the theoretical performance of the receiver calculated from Equation 2.18. The triangles correspond to the measured values of the designed receiver performance. These values are also tabulated in Table 2.

TABLE 1

Performance Measurements of the PSK Receiver

S	S+N	SNR	$\overline{X}$	σ_x	P_e
0.4	4.01	-3.6	6021.4	76.5	0.1837
0.4	3.70	-2.88	5313.28	64.09	0.1621
0.4	3.33	-1.96	4519.6	36.1	0.1379
0.4	3.0	-1.0	3322.0	37.7	0.101
0.4	2.927	0.0	3161.3	29.8	0.096
0.51	2.91	1.35	1772.4	29.9	0.054
0.59	2.92	2.675	1010.9	30.8	0.0308
0.66	2.94	3.63	599.9	19.9	0.0183
0.763	2.97	4.87	287.8	13.6	0.008782
.9	3.15	5.87	109.7	5.8	0.00334
.96	3.17	6.42	65.5	7.7	0.00199
1.1	3.20	7.65	12.8	4.4	0.00039
1.21	3.25	8.45	3.83	0.9	0.0001168
1.36	3.30	9.49	0.4	0.51	0.0000122
1.53	3.38	10.49	0.	--	--
1.81	3.51	11.97	0.	----	

TABLE 2

Performance Measurements of the PSK Receiver

SNR	P_e			
	JSR=0.5	JSR=1.0	JSR=2.0	JSR=5.0
-3.60	0.2351	0.2792	0.3426	0.4443
-2.88	0.2242	0.2753	0.3446	0.4544
-1.96	0.2124	0.2713	0.3530	0.4658
-1.00	0.1700	0.2322	0.3370	0.4686
0.00	0.1670	0.2361	0.3386	0.4711
1.35	0.1725	0.2708	0.3902	0.4939
2.68	0.1594	0.2711	0.4093	0.5000
3.63	0.1458	0.2642	0.4178	0.5000
4.87	0.1316	0.2712	0.4326	0.5000
5.87	0.1190	0.2570	0.4497	0.5000
6.42	0.1120	0.2670	0.4552	0.5000
7.65	0.0928	0.2674	0.4698	0.5000
8.45	0.0856	0.2698	0.4773	0.5000
6.42	0.1120	0.2670	0.4552	0.5000
7.65	0.0928	0.2674	0.4698	0.5000
8.45	0.0856	0.2698	0.4773	0.5000
9.49	0.0658	0.2720	0.4871	0.5000
10.49	0.0513	0.2700	0.4946	0.5000
11.97	0.0320	0.2811	0.5000	0.5000

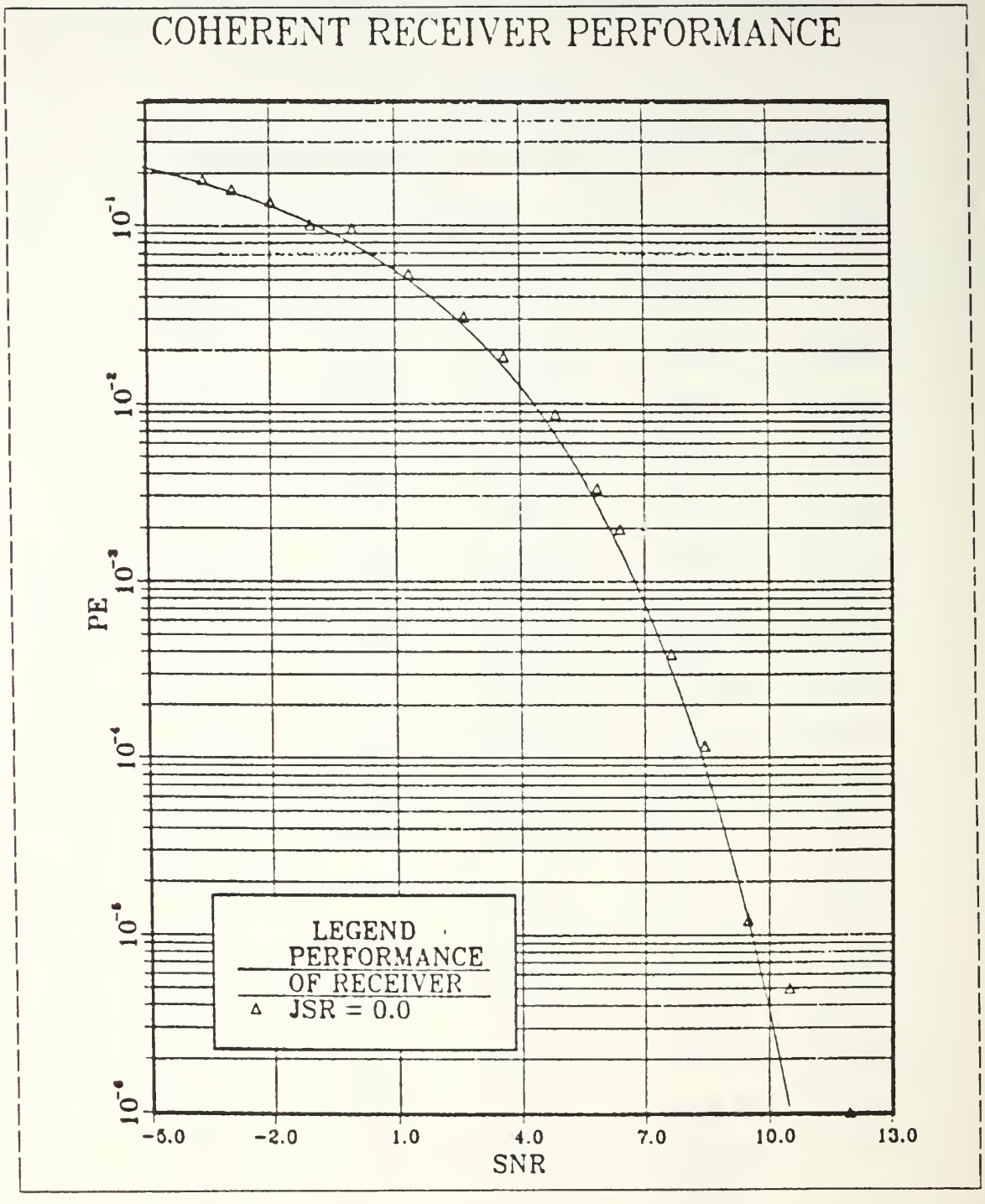

Figure 4.1 Performance of the PSK Receiver

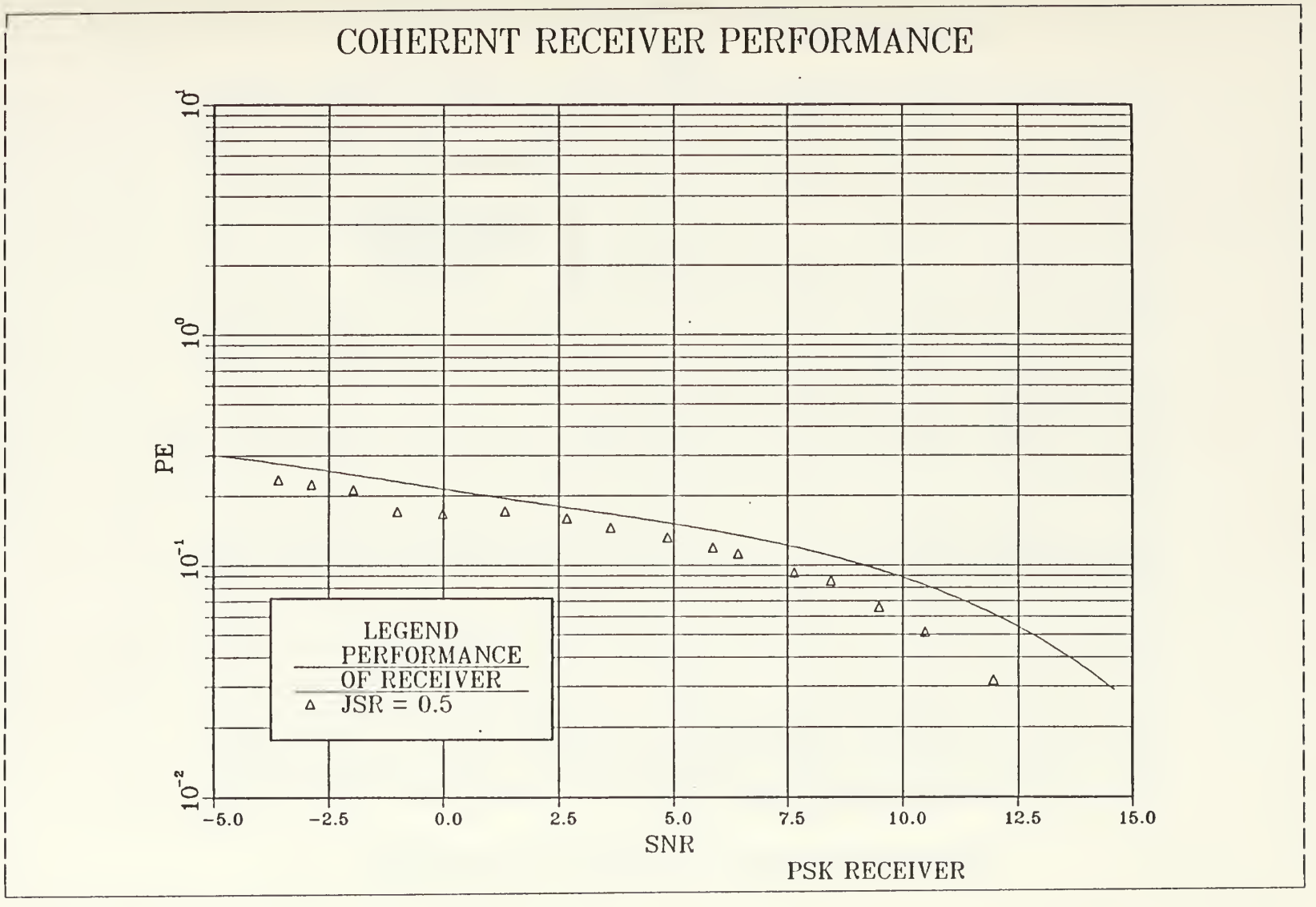

Figure 4.2 Performance of the PSK Receiver for JSR=0.5

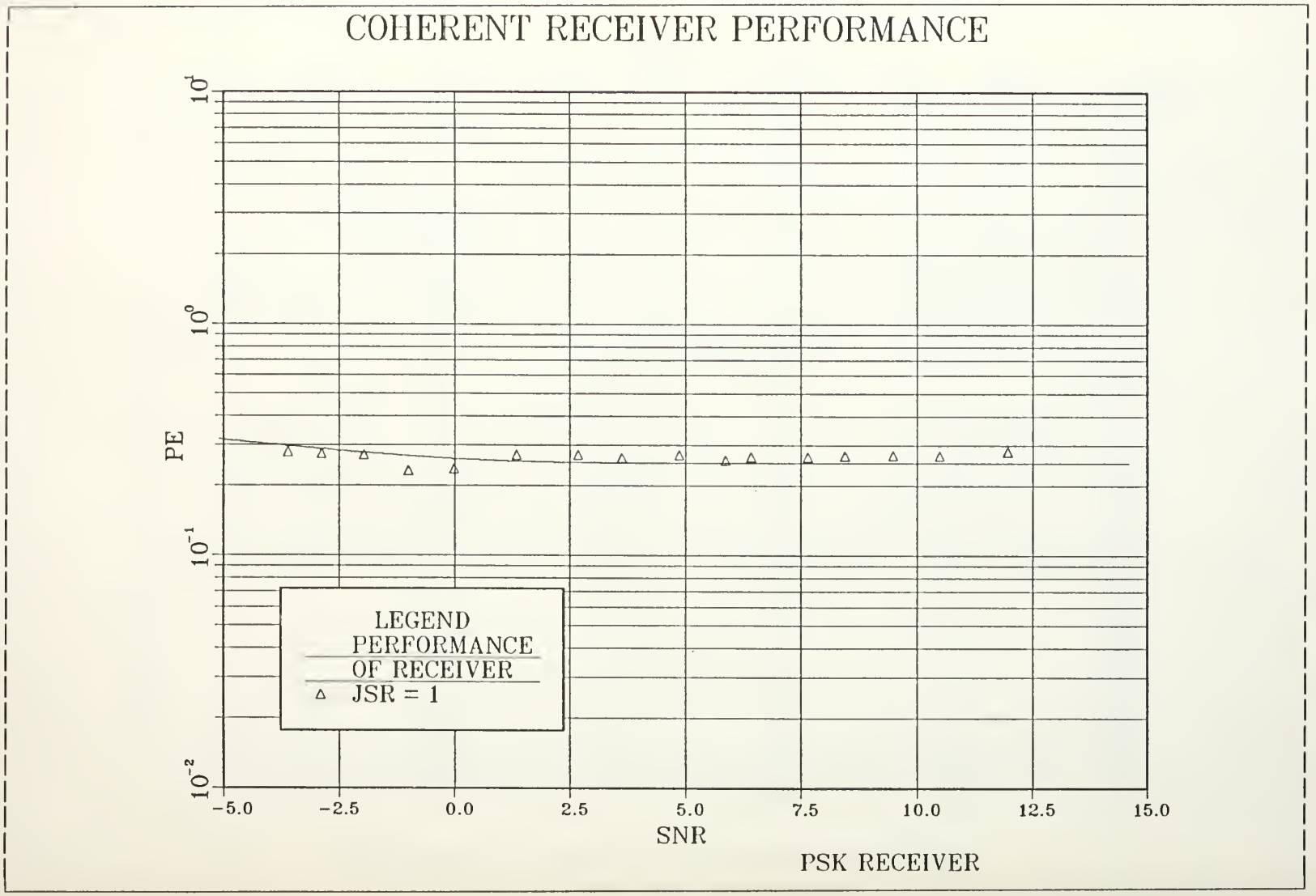

Figure 4.3 Performance of the PSK Receiver for JSR = 1.0

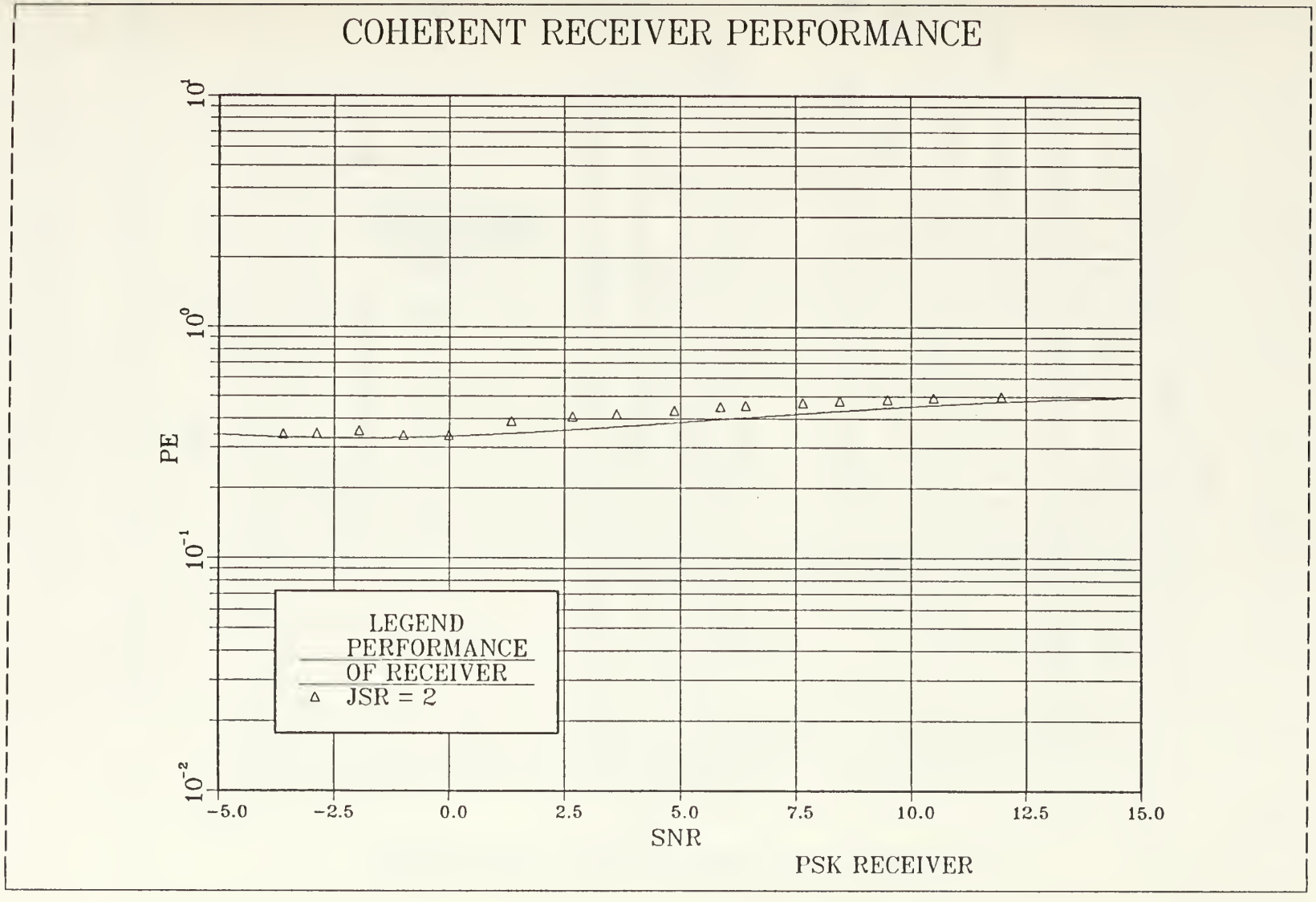

Figure 4.4 Performance of the PSK Receiver for JSR = 2.0

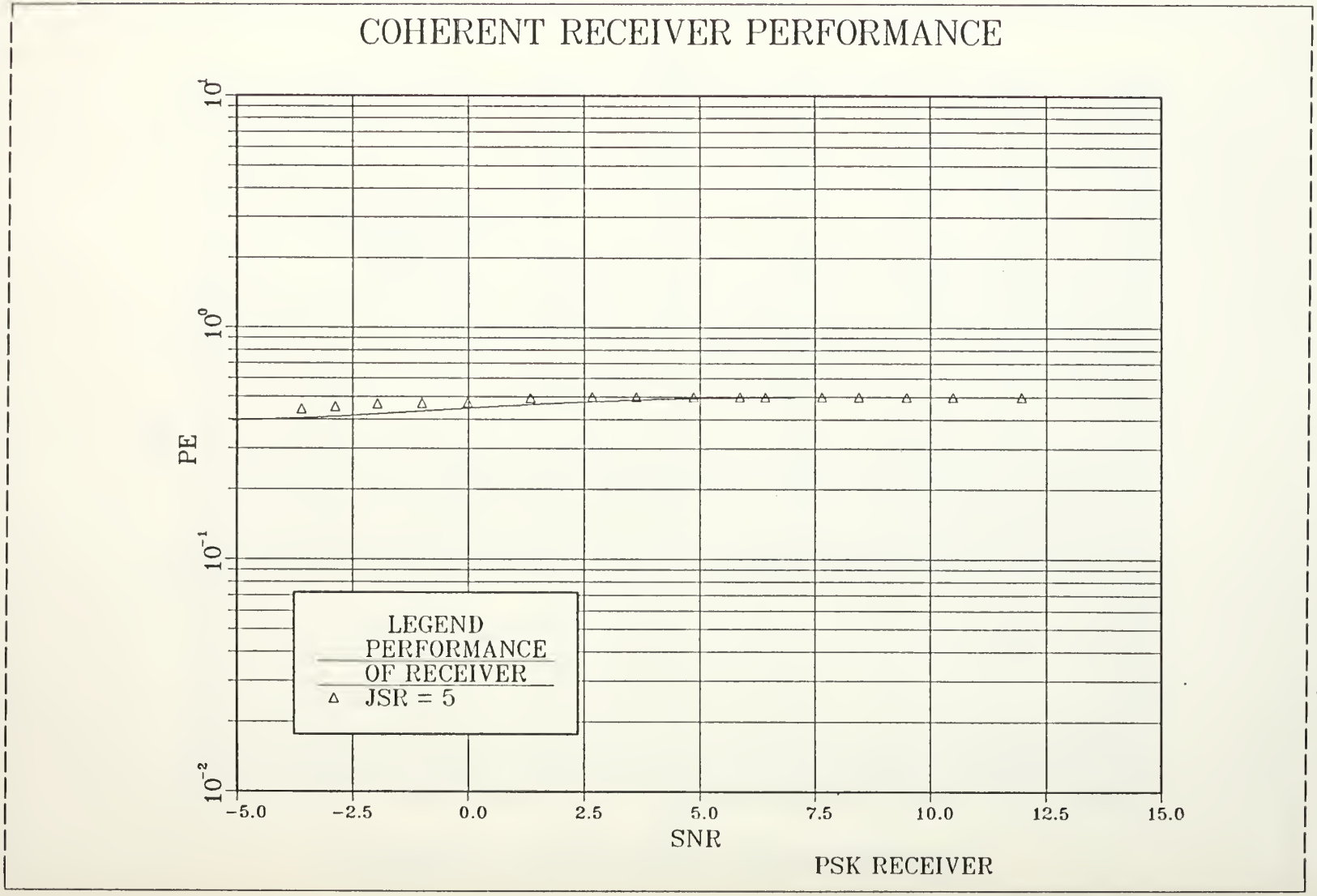

Figure 4.5 Performance of the PSK Receiver for JSR = 5.0

1. Sample Calculation

For this experiment, the transmitted message (data) is a binary bipolar waveform of amplitude +5 volts and a bit rate 2000 bits per second. The carrier waveform is a single sinusoidal tone of 20 kHz frequency and amplitude A of 5 volts. The jamming waveform is a single sinusoidal tone of the same frequency as that of the carrier (for this case 20 kHz) and amplitude adjusted to give at the receiver's input an RMS voltage such as to produce a Jammer-to-Signal ratio (JSR) equal to the examined values of 0.5, 1.0, 2.0, and 5.0.

At the input of the receiver, the RMS voltages for the cases of only signal transmitted and signal plus noise transmitted are measured as shown in Table 4.1. The calculation of Signal-to-Noise ratio is described as follows,

$$N^2 = (S+N)^2 - S^2$$

where N is the RMS voltage of the noise,

S is the RMS voltage of the signal, and

(S+N) is the RMS voltage of signal plus noise.

$$N_o = \frac{N}{BW}$$

where N_o is the level of the noise power spectrum,

and BW is the 3 dB bandwidth of the noise.

$$E_b = S^2 T_b \qquad (4.1)$$

where E_b is the energy of one data bit, and T_b is the duration of one bit.

$$SNR = E_b / N_o$$

and $$(SNR)_{dB} = 10 \log(SNR)$$

As an example, the calculations made for the first row of Table 4.1 are presented here. These result in

$$N^2 = (3.15)^2 - (0.9)^2 = 9.112$$

$$N_o = 9.112 / 87000 = 0.0001047 = 1.047 \times 10^{-4}$$

$$E = (0.9)^2 / 2000 = 0.000405 = 4.05 \times 10^{-4}$$

$$SNR = 4.05 \times 10^{-4} / 1.047 \times 10^{-4} = 3.866$$

$$(SNR)_{dB} = 10 \log(3.866) = 5.87 dB$$

Next, the number of errors that occured during the transmission of 32,768 bits is counted. After twenty such measurements, it is found that the average number of errors occurring is $\overline{X} = 109.7$ with a standard deviation of $\sigma_{\overline{x}} = 5.8$. Then, the probability of receiver error is calculated as

$$P_e = 109.7 / 32768 = 3.34 \times 10^{-3}$$

When the performance of the receiver in the presence of a jamming waveform is measured, the Jamming-to-Signal ratio is calculated by taking measurements of the RMS voltages at the input of the receiver when signal plus jamming waveform is transmitted. Then we calculate JSR as follows

$$J_I^2 = (J+S)^2 - S^2$$

where J_I, S and (J+S) are the RMS voltages of the jamming waveform, the signal, and the signal plus jammer respectively. Then

$$JSR = J_I^2 / S^2$$

where JSR is the Jammer-to-Signal ratio.

For example, when the RMS voltage of the signal is measured as 0.9 volts RMS and the RMS voltage of signal plus jammer (S+J) is measured as 1.1 volts RMS, we calculate JSR as follows

$$(J_I)^2 = (1.1)^2 - (0.9)^2 = 0.4$$

$$JSR = (J_I)^2/(S)^2 = 0.4 / 0.81 = 0.494 = 0.5$$

The performance of the receiver in terms of P_e when the data transmission is interfered by a jamming waveform, is measured and calculated as done when only signal and noise are present at the input of the receiver. This procedure is carried out as described above.

C. FSK EXPERIMENTAL RESULTS

For FSK modulation, the performance of the system in the presence of noise and the jamming waveform described in Section A of this Chapter in terms of the probability of error is calculated as the SNR changes for specified values of JSR. The results are shown in tables 4.3 and 4.4 as JSR takes on values 0.0, 0.5, 1.0, and 5.0. In Figures 4.6 through 4.10 the probability of error (P_e) versus SNR is plotted for the corresponding values of JSR.

In Figure 4.6 the performance of the receiver is plotted when the transmitted signal is interfered by noise only. The theoretical performance of the receiver which is calculated from Equation 2.12. is plotted with the solid line. The experimentally measured performance of the designed receiver is plotted using the small triangles. These measured values of the receiver performance are also presented in Table 3.

In Figures 4.7 through 4.10, the performance of the receiver is plotted when the transmitted signal is interfered by noise as well as by the jamming waveform previously described. Each of the Figures corresponds to a specific value of JSR as shown in the legend. The solid line represents the theoretical performance of the receiver calculated from Equation 2.19. The small triangles correspond to the

measured values of the designed receiver performance. These values are also shown in Tables 4 and 5 for the corresponding values of JSR.

1. Sample Calculation

For this experiment, the transmitted message is a binary waveform of amplitude 5 volts and a bit rate 2000 bits per second. The frequencies usd are 20 kHz for f_0 and 32 kHz for f_1 so that no significant overlapping of the signal sidelobes can occur. (Note that each sidelobe occupies bandwidth of 2 kHz).

The amplitude of each of the carriers is 5 volts. The jamming waveform is the difference of the two carrier waveforms, with amplitude adjusted to give at the receiver's input an RMS voltage such as to produce a Jammer-to-Signal ratio having values of 0.5, 1.0, 2.0, and 5.0.

The rest of the calculations for this case are exactly the same as those carried out for the PSK case described previously in this chapter.

D. COMPARISON OF EXPERIMENTAL WITH THEORETICAL RESULTS.

The theoretical performance of the receiver in terms of the probability of error is presented in Chapter II. In Figures 4.1 through 4.10, the theoretical performance of the

TABLE 3

Performance Measurements of the FSK Receiver

S	S+N	SNR	$\bar{X}$	σ_x	P_e
0.409	4.56	-4.54	9344.8	42.1	0.285
0.409	4.00	-3.37	8466.9	72.7	0.258
0.41	3.5	-2.20	7408.8	64.6	0.226
0.41	3.12	-1.18	6530.2	48.7	0.199
0.40	2.69	0.0	5712.9	65.8	0.174
0.45	2.70	1.0	4588.6	48.32	0.140
0.51	2.71	2.0	3683.1	48.08	0.112
0.56	2.72	2.80	3250.4	40.8	0.0991
0.647	2.74	4.10	2235.3	50.5	0.0682
0.72	2.7	5.02	1589.5	36.2	0.0480
0.797	2.78	5.91	1090.2	32.3	0.0332
0.902	2.81	6.97	636.4	23.09	0.0194
1.0	2.84	7.89	326.9	23.9	0.00997
1.14	2.89	9.04	157.1	11.96	0.00479
0.42	0.98	9.91	86.09	13.12	0.00262
0.48	1.00	11.15	22.11	5.7	0.000674
0.54	1.04	12.06	4.9	2.2	0.000149

TABLE 4

Performance Measurements of the FSK Receiver

JSR=0.5		JSR=1.0	
SNR	P_e	SNR	P_e
-4.81	0.3240	-3.57	0.340
-3.93	0.3130	-2.40	0.339
-2.98	0.3029	-1.04	0.343
-2.10	0.2940	-0.07	0.330
-1.00	0.2596	0.94	0.337
0.70	0.2510	4.20	0.372
2.03	0.2440	3.01	0.351
2.93	0.2410	1.87	0.344
4.28	0.2380	12.06	0.468
5.00	0.2380	11.04	0.459
5.97	0.2389	13.20	0.483
7.00	0.2380	9.91	0.440
7.92	0.2381	14.50	0.497
9.03	0.2391	15.70	0.500
10.04	0.2065	5.02	0.383
11.38	0.2080	5.94	0.404
12.99	0.2120	6.97	0.413
14.40	0.2099	7.81	0.432
15.40	0.2020	8.97	0.452
16.90	0.2030	16.98	0.500

TABLE 5

Performance Measurements of the FSK Receiver

SNR	P_e	
	JSR=2.0	JSR=5.0
-4.19	0.3860	0.4590
-3.27	0.3920	0.4690
-1.99	0.4010	0.4810
-0.99	0.4140	0.4900
0.97	0.4230	0.4970
1.70	0.4360	0.5000
3.00	0.4560	0.5000
4.28	0.4710	0.5000
5.00	0.4820	0.5000
5.96	0.4900	0.5000
7.00	0.4960	0.5000
7.92	0.4990	0.5000
9.03	0.5000	0.5000
9.91	0.5000	0.5000
11.04	0.5000	0.5000
12.06	0.5000	0.5000
13.20	0.5000	0.5000
14.50	0.5000	0.5000
15.70	0.5000	0.5000
16.90	0.5000	0.5000

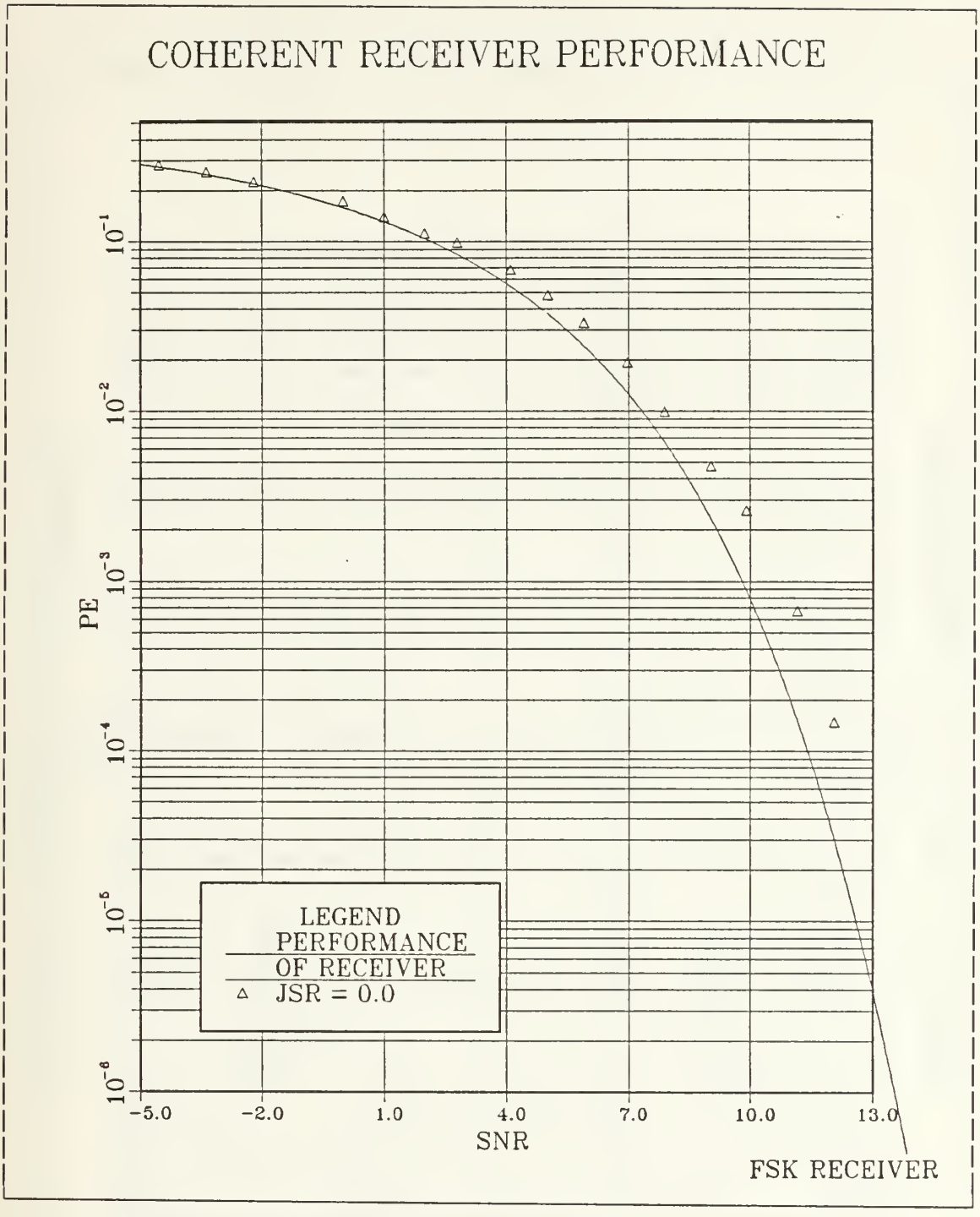

Figure 4.6 Performance of the FSK Receiver

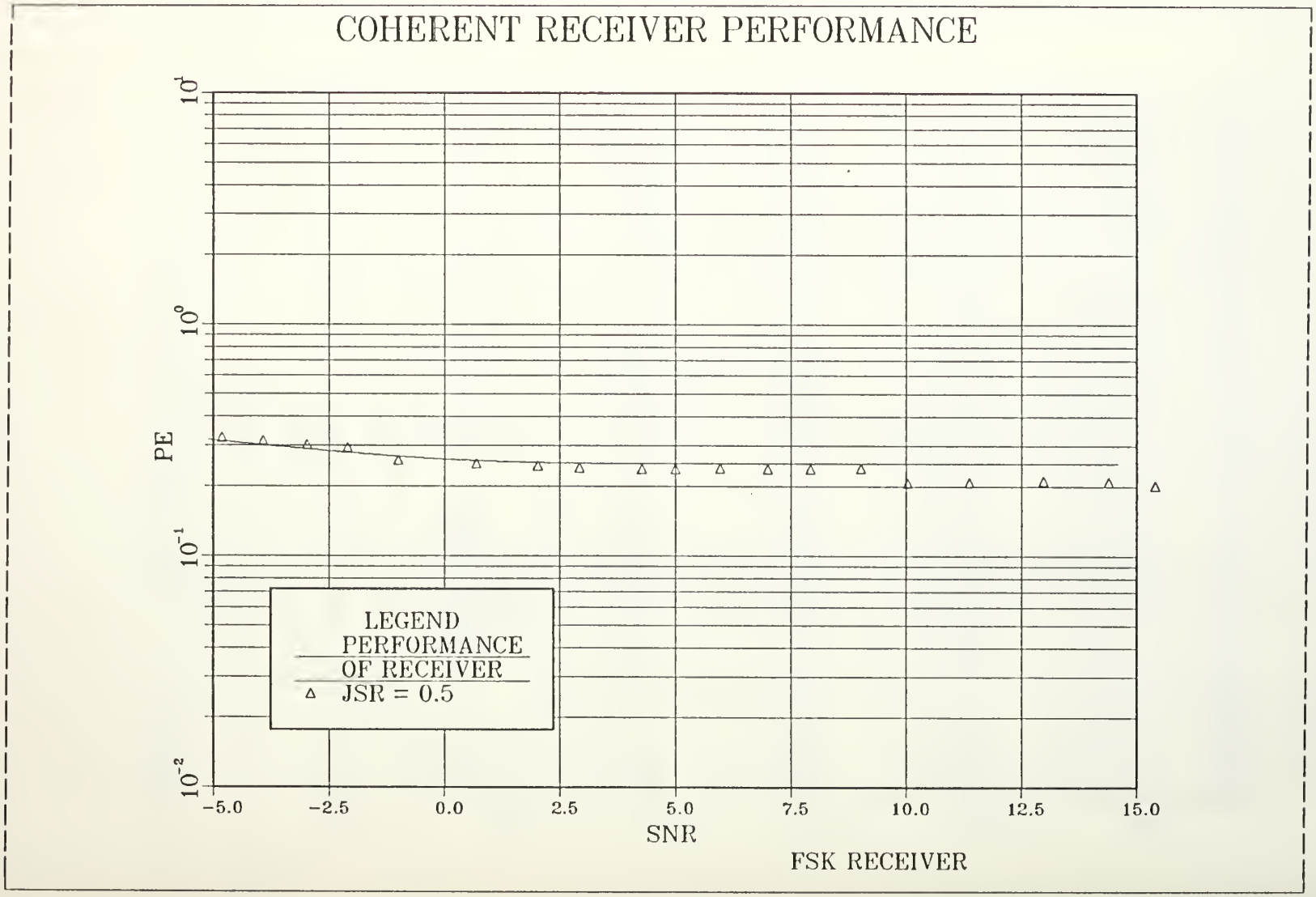

Figure 4.7 Performance of the FSK Receiver for JSR=0.5

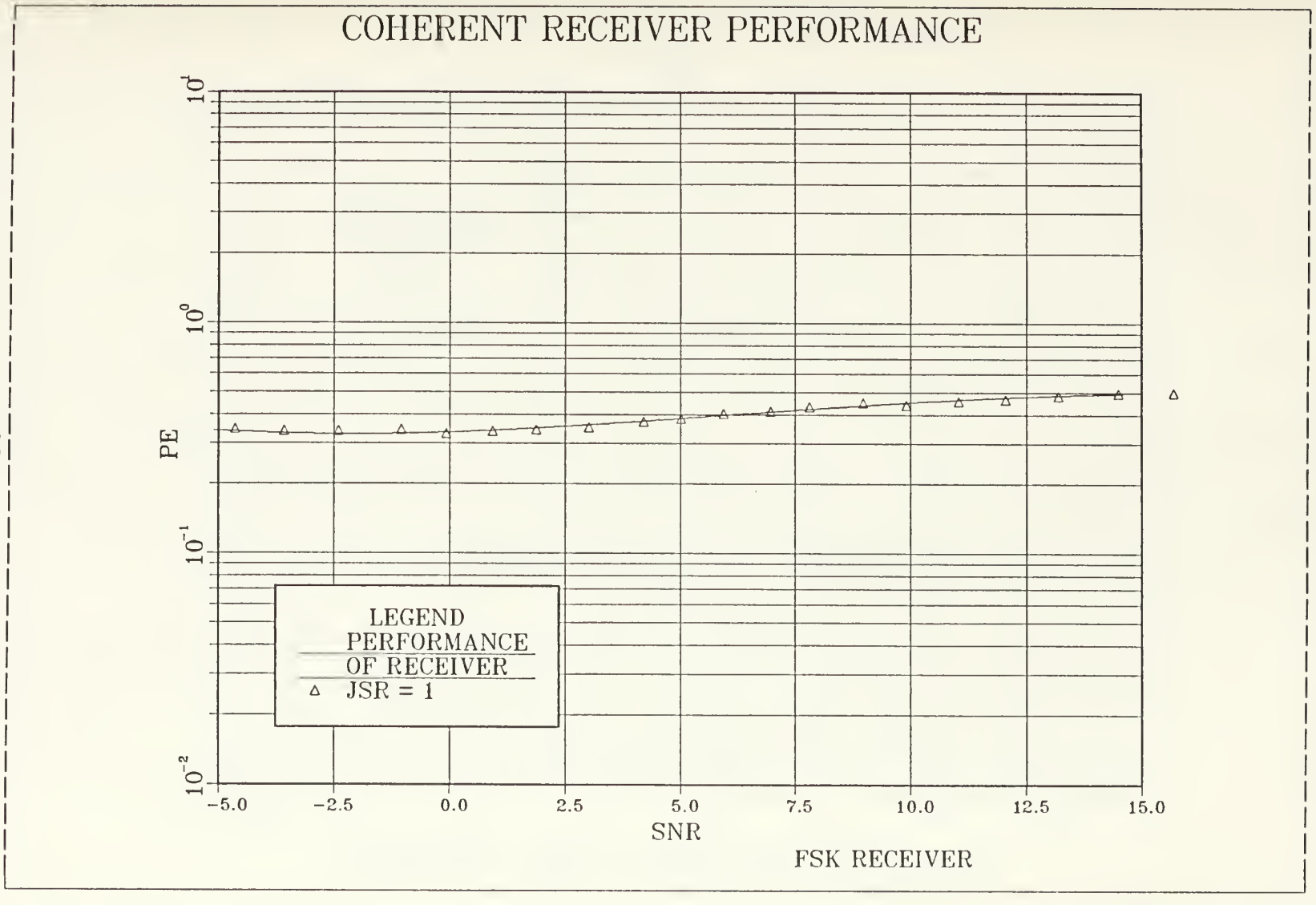

Figure 4.8 Performance of the FSK Receiver for JSR = 1.0

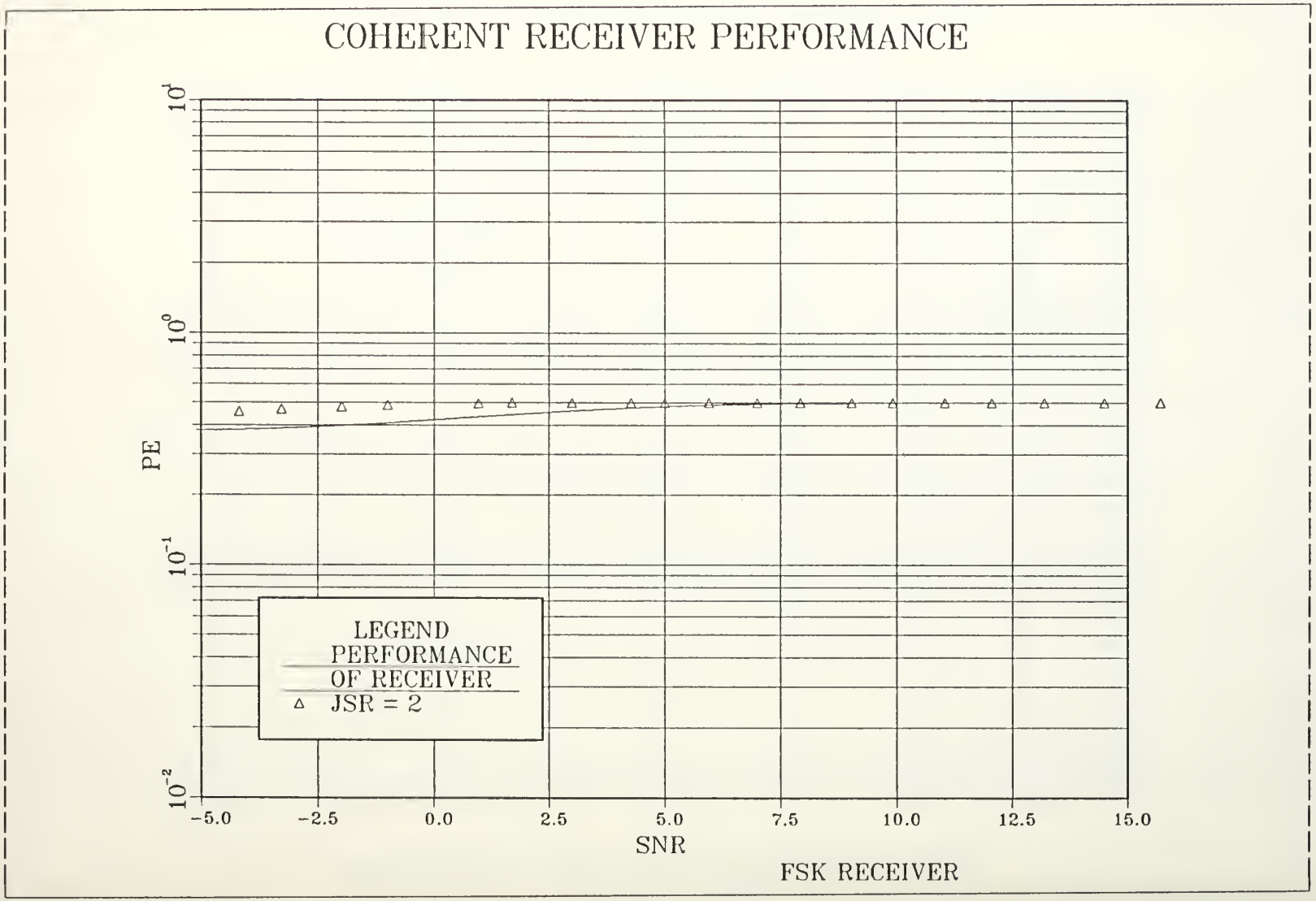

Figure 4.9 Performance of the FSK Receiver for JSR = 2.0

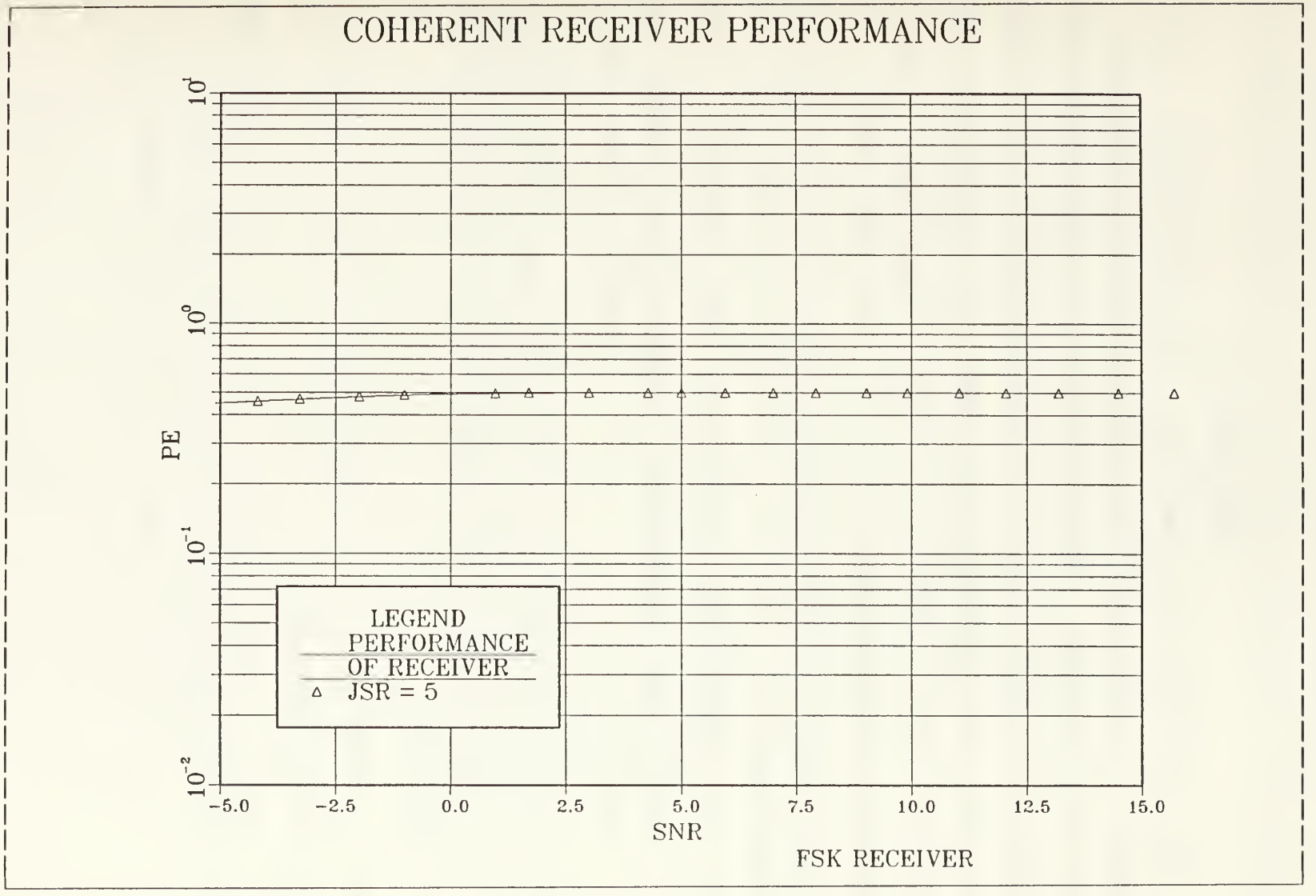

Figure 4.10 Performance of the FSK Receiver for JSR = 5.0

receiver is plotted versus SNR with JSR as parameter, together with the experimental results, that is the measured P_e.

The agreement with the theory is obvious from these figures. Furthermore, it can be observed that the experimental results reach but generally do not exceed the theoretical performance levels. Certain inferior experimental results can be explained by the fact that assumptions made in the derivation of the performance of the receiver cannot be fullfilled in practice.

Main reasons for the reduced measured performance of the receiver are:

1. The integration interval of the integrators is smaller than theoretically required by a factor of about 5%.

2. The orthogonality of the signals cannot be guaranteed as the frequency adjustments of the sources are made manually.

3. Instability of the signal sources, and the accuracy of the instruments.

4. Errors in the measurement of the noise bandwidth and the resulting error in the calculation of N_o.

V. CONCLUSIONS

The application of results derived in the statistical communication theory literature are presented in this thesis. The performance of a digital receiver in terms of the probability of receiver error is examined when the receiver operates in the presence of additive Gaussian noise and a jamming waveform. Two different systems are examined separately, one for binary Phase Shift Key modulation and the other for binary Frequency Shift Key modulation techniques. For both, the results of the experimental work are very close to known theoretical results as demonstrated in greater detail in Chapter IV.

The structure of the receiver proposed by statistical communication theory results is verified here to operate at the predicted performance levels. Of course, because idealized mathematical operations are difficult to implement with circuits having finite tolerances, the performance of the designed circuits is not exactly as that predicted by the theory.

For this work, the performance of the receiver operating in the presence of an "optimum" jammer is examined.

A major thrust of this thesis was to investigate and experimentally validate results derived analytically on the performance of binary receivers operating in the presence of noise and jamming. The transmission signals, the noise and the jamming waveforms have been simulated, receivers have been built, their performance measured, and in each case, it has been found that the measured performance very closely tracks the performance predicted by earlier analysis.

A proposal for future work in this area is the examination of the performance of the receiver when different jamming waveforms are present during the transmission of a binary message using Phase Shift Key and Frequency Shift Key modulation techniques. Also some other modulation techniques not examined in this work, such as Amplitude Shift Key or On-Off Key can be a topic for future work. Finally, work on noncoherent receivers operating in a jamming environment can be studied and experimentally analyzed in a manner similar to that carried out in this thesis.

APPENDIX A

SCHEMATIC DIAGRAMS OF DESIGNED CIRCUITS

In the schematic diagrams of this Appendix, the values of all resistors are in kilo Ohms, and the values of capacitors in micro Farad.

Pins not shown are not connected.

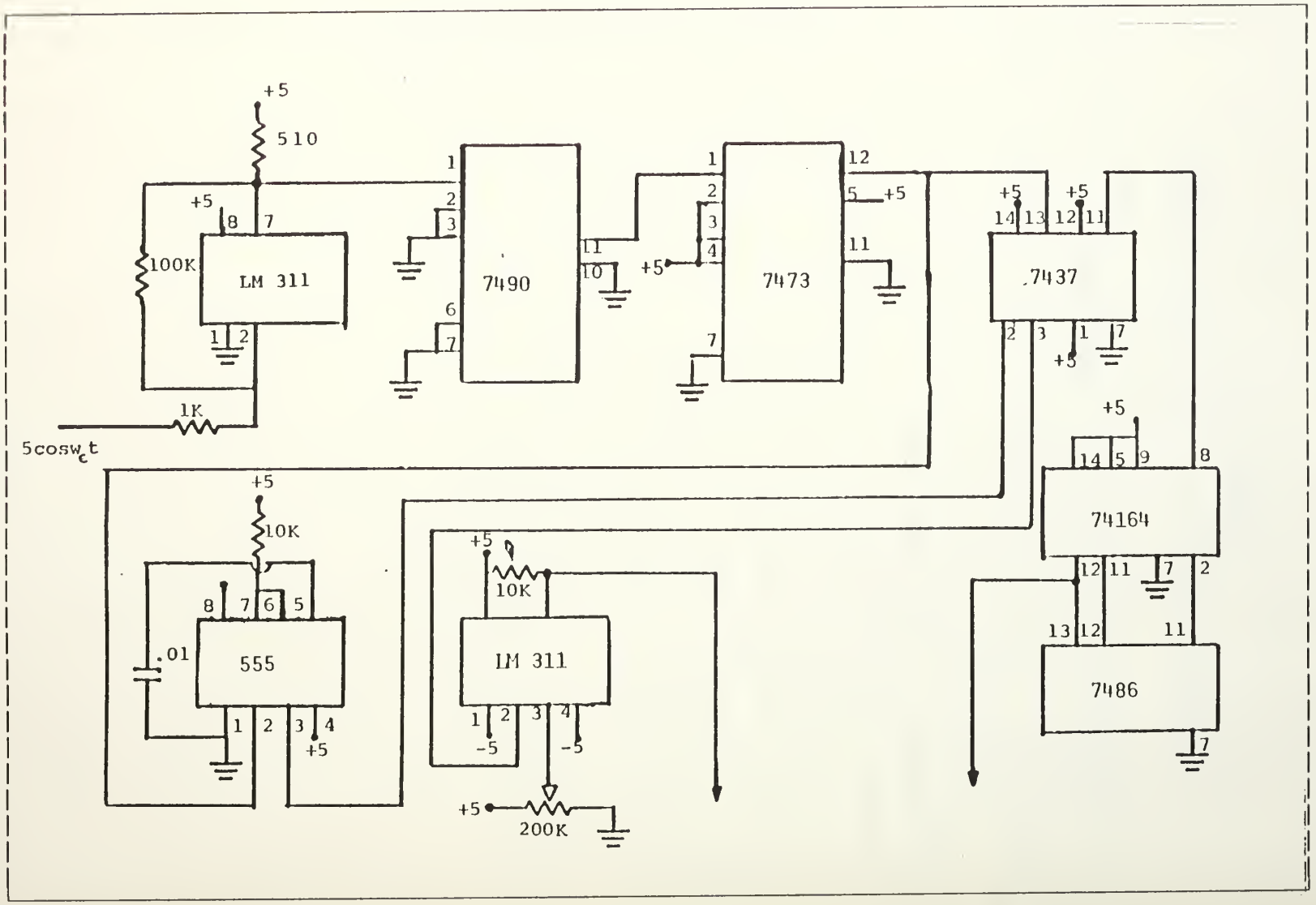

Figure A.1 Signal Generating Circuit Diagram

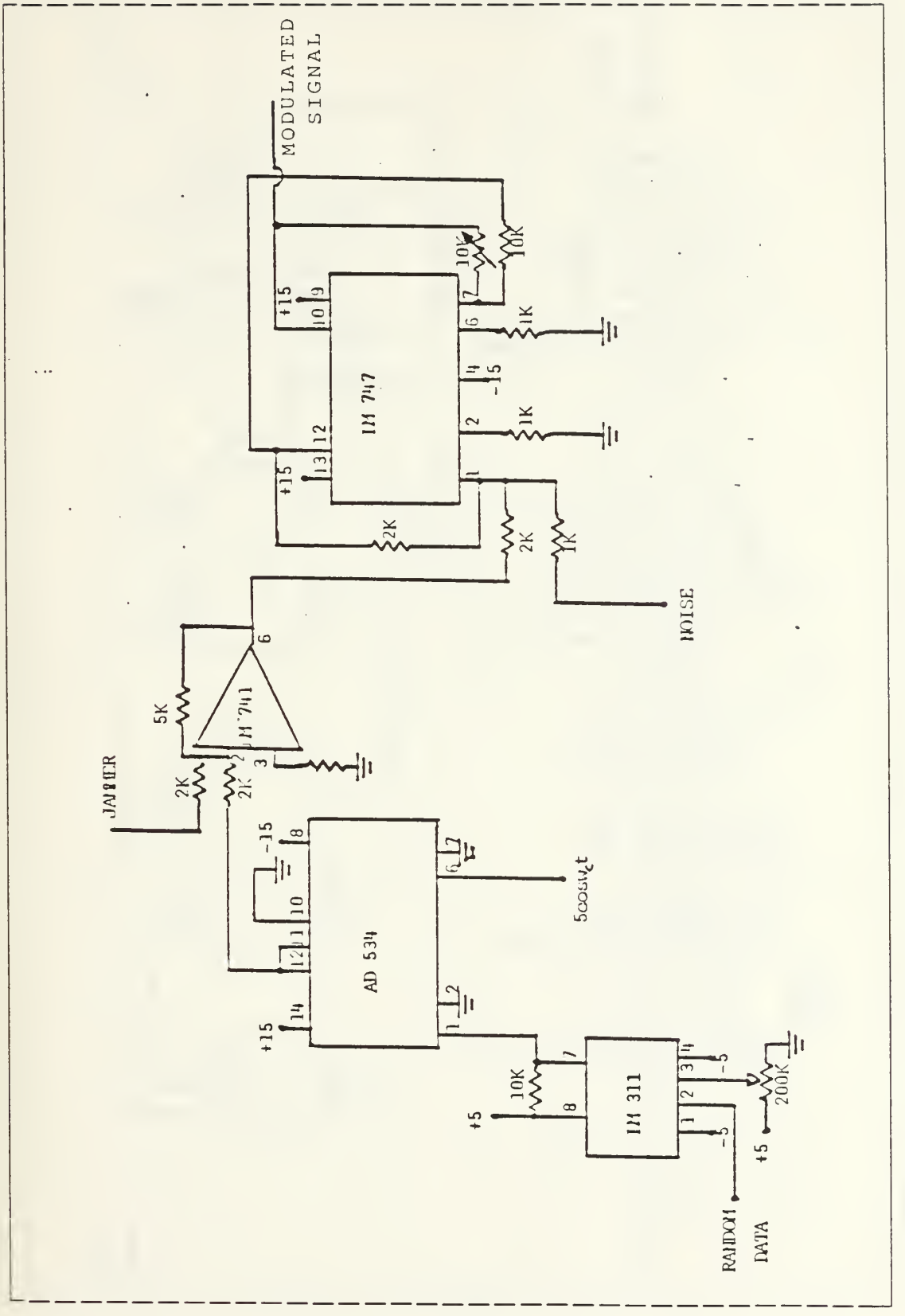

Figure A.2 PSK Modulator Diagram

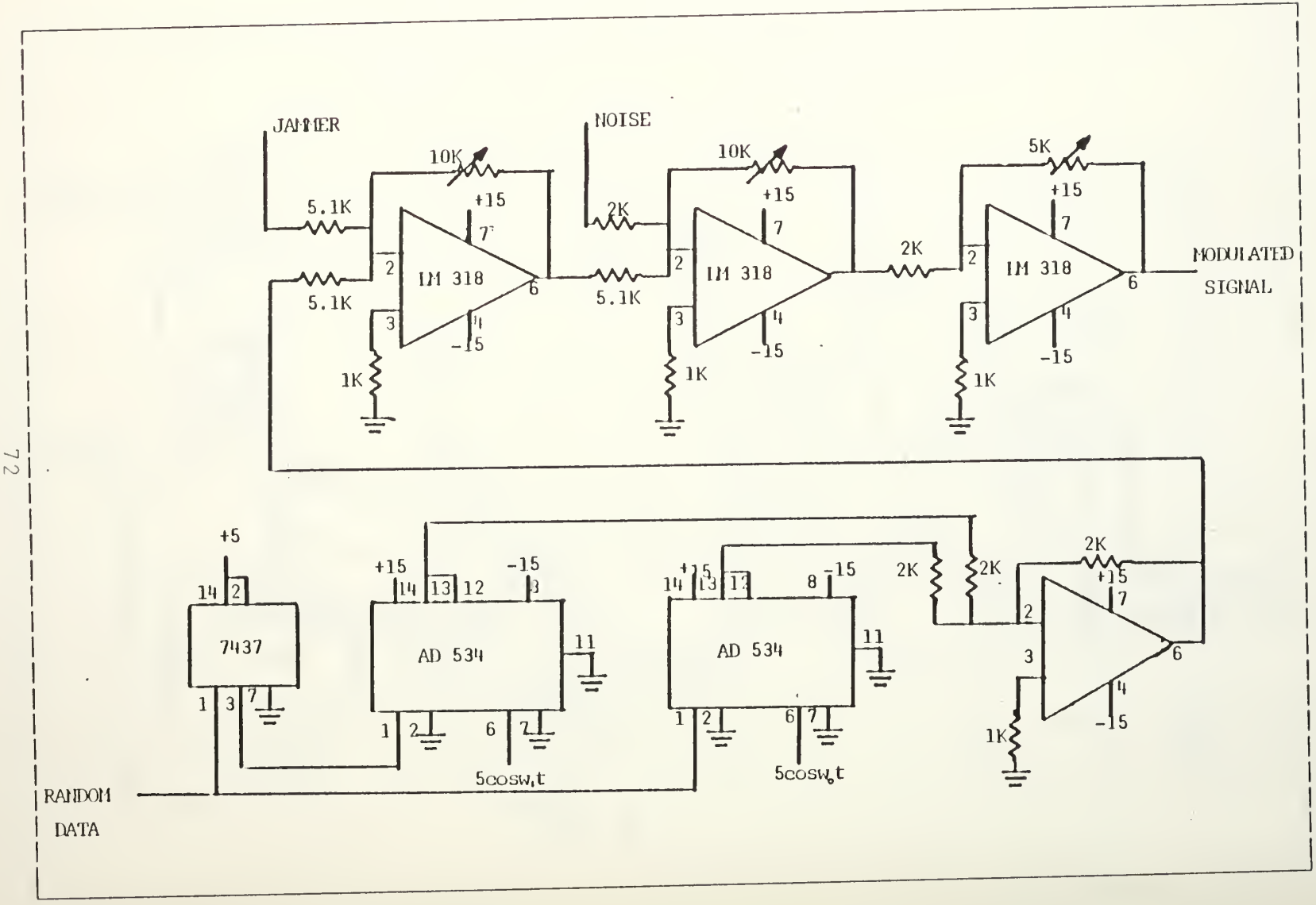

Figure A.3 FSK Modulator Diagram

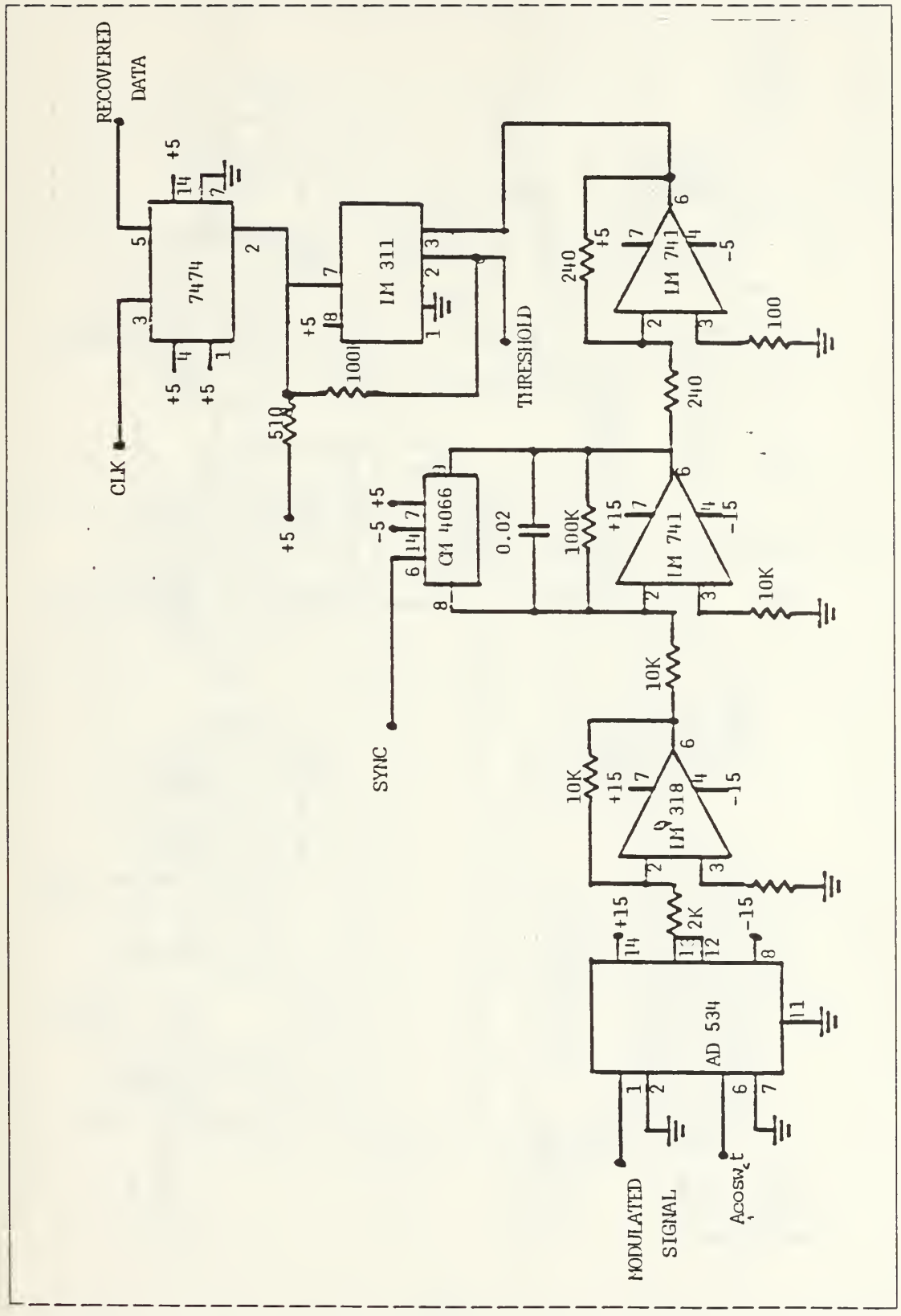

Figure A.4 PSK Receiver Diagram

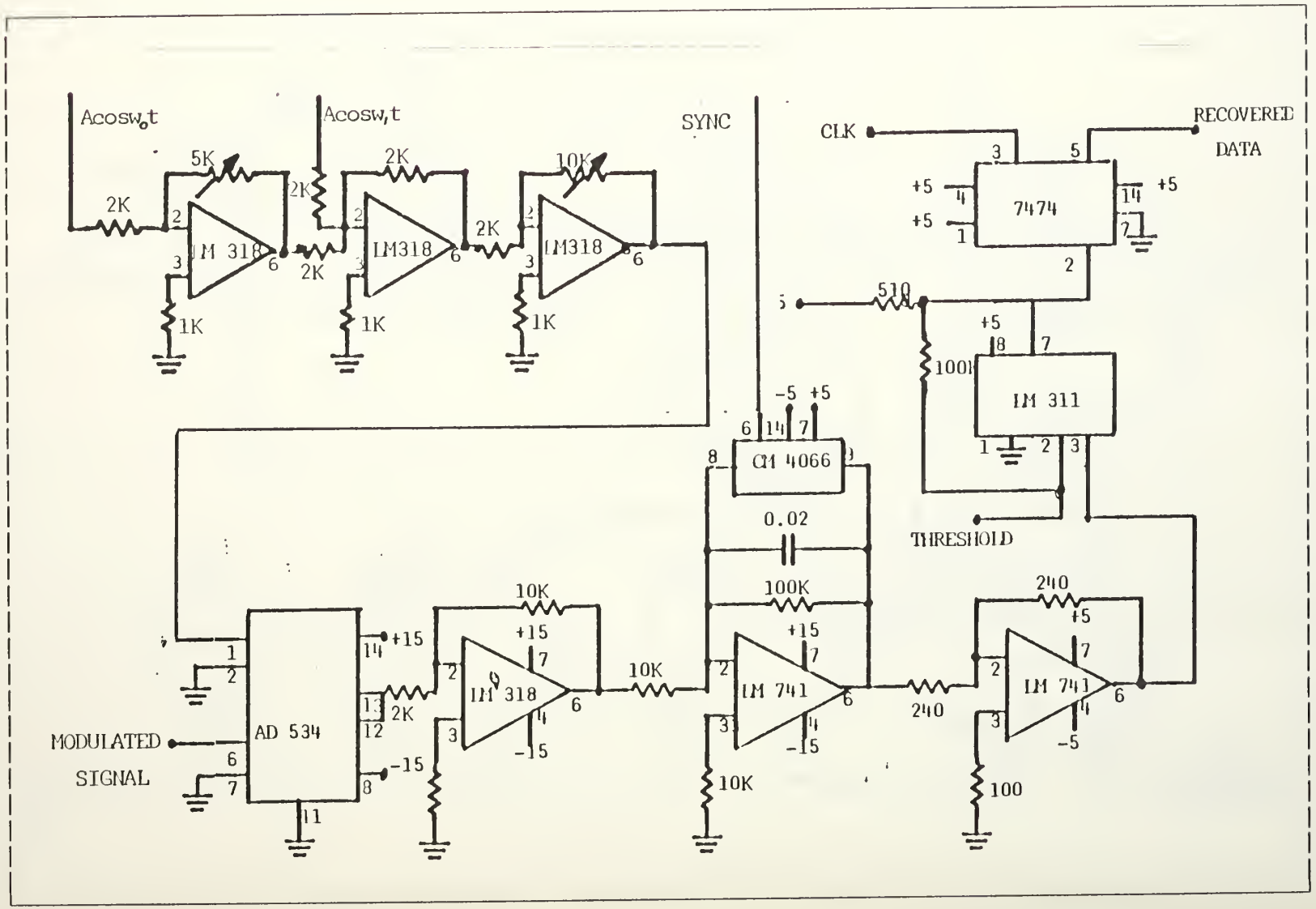

Figure A.5 FSK Receiver Diagram

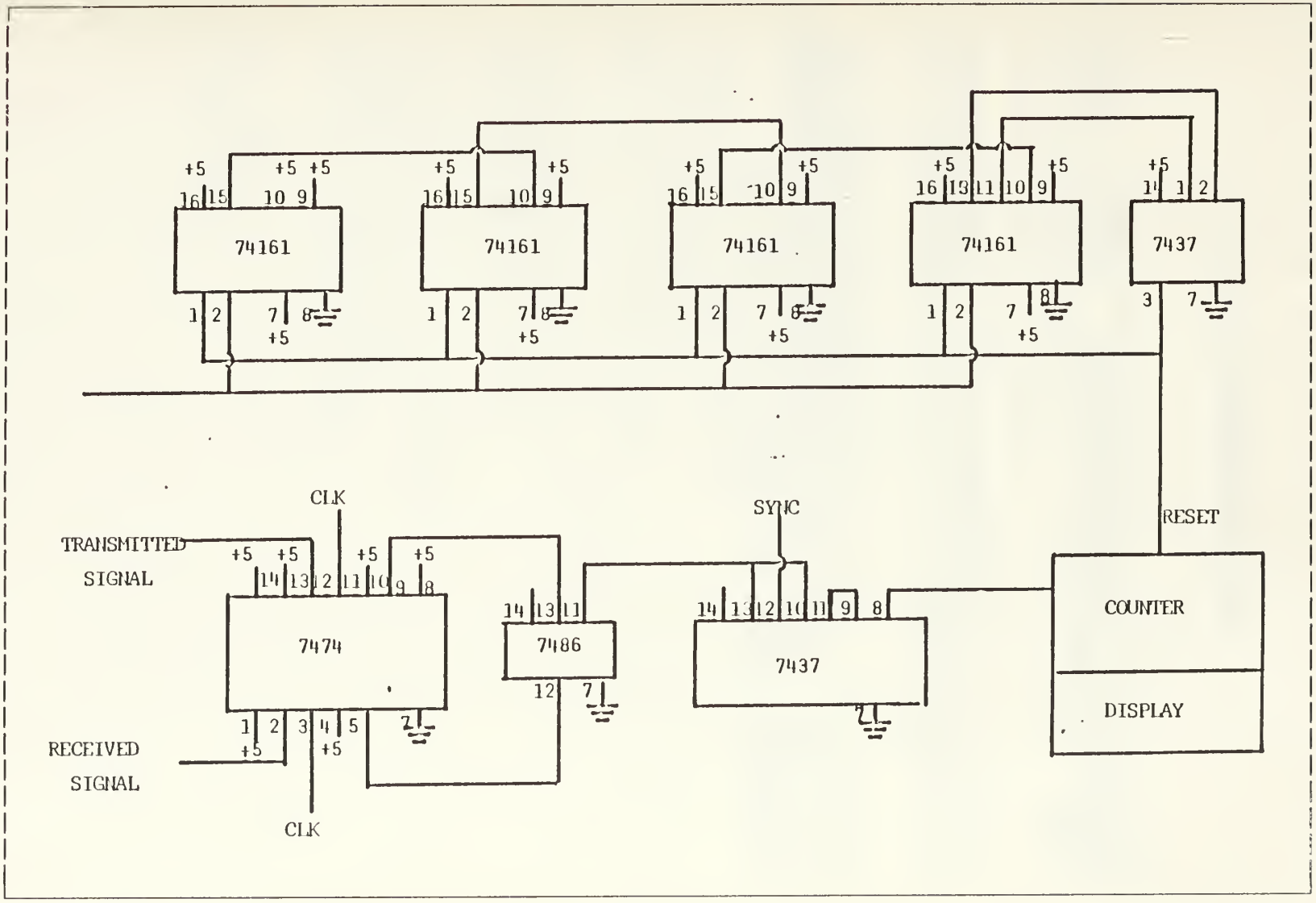

Figure A.6 Counting Circuit Diagram

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2. Srinath, M. D., Rajasekaran, P. K. An Introduction to Statistical Signal Processing with Applications, John Wiley & Sons, 1979.

3. Bukofzer, D. Final Report for Research Contract No. 5156-5160. Performance of Optimum and Suboptimum Incoherent Digital Communication Receivers in the Presence of Noise and Jamming", February 1984.

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